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THESIS

DEVELOPMENT OF AN NPS MIDDLE ULTRAVIOLET SPECTROGRAPH (MUSTANG) ELECTRONIC INTERFACE PACKAGE

by

John H. Quint

December, 1991

Thesis Advisor: David D. Cleary

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19 Abstract *(continue on reverse if necessary and identify by block number)*

THIS THESIS DEVELOPED A ROBUST ELECTRONIC INTERFACE PACKAGE FOR THE NAVAL POSTGRADUATE SCHOOL (NPS) MIDDLE ULTRAVIOLET SPECTROGRAPH (MUSTANG) EXPERIMENT. THE MUSTANG INSTRUMENT WAS DESIGNED TO OBSERVE ATMOSPHERIC EMISSIONS IN THE 1800Å TO 3400Å WAVELENGTH REGION. MUSTANG HAS FLOWN ALONG WITH A NAVAL RESEARCH LABORATORY (NRL) INSTRUMENT ON A NASA SOUNDING ROCKET EXPERIMENT, AND IS SCHEDULED TO FLY ON TWO MORE SOUNDING ROCKETS PRIOR TO INTEGRATION ON AN AIR FORCE SATELLITE. DATA FROM THESE EXPERIMENTS WILL TEST A NEW TECHNIQUE FOR MEASURING GLOBAL IONOSPHERIC ELECTRON DENSITIES ON A REAL-TIME BASIS. THE ELECTRONIC INTERFACE LINKS THE MUSTANG INSTRUMENT WITH THE AYDIN VECTOR MMP-600 SERIES PULSE CODE MODULATION ENCODER IN THE SOUNDING ROCKET TELEMETRY SECTION. ANALOG DATA FROM MUSTANG IS DIGITIZED AND BUFFERED IN THE ELECTRONIC INTERFACE TO SUPPORT ASYNCHRONOUS TRANSFER TO TELEMETRY.

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DIGITIZED MUSTANG DATA IS TELEMETERED TO A GROUND STATION DURING ROCKET FLIGHT. THIS ELECTRONIC INTERFACE CIRCUIT WAS THOROUGHLY TESTED DURING PAYLOAD INTEGRATION WITH NASA. GROUND SUPPORT EQUIPMENT (GSE) WAS EXTENSIVELY REVISED TO SUPPORT THE MUSTANG INSTRUMENT DURING LABORATORY CALIBRATION AND LAUNCH SITE TESTING.

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DEVELOPMENT OF AN NPS MIDDLE ULTRAVIOLET SPECTROGRAPH (MUSTANG) ELECTRONIC INTERFACE PACKAGE

by

John H. Quint
Lieutenant, United States Navy
B.S., United States Naval Academy, 1984

Submitted in partial fulfillment of the
requirements for the degree of

ELECTRICAL ENGINEER
[and Master of Science in Electrical Engineer]
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ABSTRACT

This thesis developed a robust electronic interface package for the Naval Postgraduate School (NPS) Middle Ultraviolet Spectrograph (MUSTANG) experiment. The MUSTANG instrument was designed to observe atmospheric emissions in the 1800Å to 3400Å wavelength region. MUSTANG has flown along with a Naval Research Laboratory (NRL) instrument on a NASA sounding rocket experiment, and is scheduled to fly on two more sounding rockets prior to integration on an Air Force satellite. Data from these experiments will test a new technique for measuring global ionospheric electron densities on a real-time basis. The electronic interface links the MUSTANG instrument with the Aydin Vector MMP-600 Series Pulse Code Modulation Encoder in the sounding rocket telemetry section. Analog data from MUSTANG is digitized and buffered in the electronic interface to support asynchronous transfer to telemetry. Digitized MUSTANG data is telemetered to a ground station during rocket flight. This electronic interface circuit was thoroughly tested during payload integration with NASA. Ground Support Equipment (GSE) was extensively revised to support the MUSTANG instrument during laboratory calibration and launch site testing.

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LIST OF ABBREVIATIONS

A/D	Analog-to-Digital Converter
CAD	Computer Aided Design
CMOS	Complementary Metal-Oxide-Silicon Integrated Circuit
D/A	Digital-to-Analog Converter
DC	Direct Current
DIO	Digital Input/Output Interface Board
DMA	Direct Memory Access
DoD	Department of Defense
EPROM	Erasable Programmable Read Only Memory
FIFO	First-In-First-Out Memory Device
FL/RT	First Load/Retransmit Input Pin on FIFO Device
GSE	Ground Support Equipment
HCDT	Hooked Conductance Transistor
HF	High Frequency
HIRAAS	High Resolution Airglow and Aurora Spectrograph, Naval Research Laboratory Ionospheric Physics Instrument
HV	High Voltage Section of NASA Sounding Rocket
IDT	Integrated Device Technologies Corporation
I/O	Input/Output
LSB	Least Significant Bit
MCP	Microchannel Plate
MIO	Multifunction Analog, Digital, and Timing Input/Output Interface Board

MSB	Most Significant Bit
MUSTANG	Middle Ultraviolet Spectral Analysis of Nitrogen Gases, Naval Postgraduate School Ionospheric Physics Instrument
NASA	National Aeronautics and Space Administration
NB	NuBus Interface Port on Apple Macintosh
NI	National Instruments Corporation
NPS	Naval Postgraduate School
NRL	Naval Research Laboratory
PCB	Printed Circuit Board
PCD	Plasma Coupled Device
PCM	Pulse Code Modulation
RAM	Random Access Memory
RTSI	Real-Time System Integration
T/M	Telemetry Section of NASA Sounding Rocket
TTL	Transistor-Transistor-Logic Integrated Circuit
UV	Ultraviolet
VI	Virtual Instrument in LabVIEW Software
XI	Expansion In Input Pin on FIFO Device

ACKNOWLEDGEMENT

I consider it both a privilege and a pleasure to have become involved with the MUSTANG experiment. I leave this project with the deepest respect and highest regard for those scientists involved in the area of government research. Their ingenuity, optimism and dedication in pushing out the edge of the technology envelope in scientific research is to be commended. I am indebted to a large number of people for the successful completion of this design research. First, I would like to thank *Dave Rigmaiden* for his countless hours of schooling me in the areas of MILSTD and flight grade components, flight quality construction, general electronic techniques and printed circuit board layout and fabrication. I would have been lost without his guidance. He should write a book.

Next, I am indebted to *Glenn Harrell* for his precision construction of the flight enclosure for the interface circuit. He did a professional job for us on very short notice. I am equally indebted to *George Jaksha* who has professionally machined numerous parts and components in support of the MUSTANG project from the very beginning. I truly believe that he can make anything. *Dale Galarowicz* assembled the flight circuit boards and wiring harness. He is possesses an unimaginable wealth of electronic knowledge which I tapped on numerous occasions.

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I. INTRODUCTION

The MUSTANG instrument was developed at the Naval Postgraduate School in response to a research requirement for defense environmental satellites put forth by the Joint Chiefs of Staff. Reference 1, the Joint Chiefs of Staff Memorandum MJCS 154-86, was published on March 21, 1986. It listed *Measurement of the Electron Density of the Earth's Ionosphere* as the fifth highest priority research area out of 50 research requirements. Development of many modern high frequency (HF) military systems requires an accurate knowledge of ionospheric electron densities. HF electromagnetic waves used by these military systems are reflected and bent by the ionosphere. Research is presently being conducted to relate knowledge of the ionospheric electron density to the following areas.

- High Frequency Radio Communications
- Over-The-Horizon Radar Systems
- Ballistic Missile Early Warning Systems
- Ground Wave Emergency Network

Current electron density measurements of the ionosphere are made from ground-based radar systems or ionosonde stations. These measurements do not give a global picture of the ionosphere composition. The ideal measurement platform would be based on a satellite where constant observations can be taken. A spaced-based ionosonde measurement platform is impractical due to size and power restrictions. A passive measurement platform is necessary for satellite based observations.

Scientists at the Naval Research Laboratory (NRL) and the Naval Postgraduate School (NPS) are working on passive methods of measuring the electron density of the ionosphere. They currently believe that by measuring specific atmospheric emissions, they can infer ionospheric electron densities from photochemical models of the ionosphere. Reference 2 provides more information on this work.

The NRL HIRAAS instrument is a Rowland Circle Spectrograph which provides passive measurement of the ionosphere in the 500Å to 1500Å wavelength region. The NPS MUSTANG instrument is an Ebert-Fastie Middle Ultraviolet Spectrograph which provides passive measurement of the ionosphere in the 1800Å to 3400Å wavelength region. The two instruments together have been successfully launched on the National Aeronautics and Space Administration (NASA) rocket experiment number 36.053DE in March of 1990. The two-stage Terrier-Black Brant launch vehicle was launched with the two instruments from White Sands Missile Range in New Mexico. HIRAAS data was recorded on electrographic film during flight, and MUSTANG data was telemetered to a ground station. Observations were made from an altitude of 100 to 320km and the data recovered were excellent.

The success of this rocket flight led to the scheduling of an additional flight on NASA rocket experiment number 36.088DE to launch in February 1992. Additionally, a contract has recently been awarded for an Air Force satellite, P91-1,which will carry HIRAAS and MUSTANG into low earth orbit to make ionospheric observations from space for at least a year. The satellite is to be launched in the Fall of 1995.

Several changes and modifications to the MUSTANG instrument were necessary to prepare it for the next NASA sounding rocket launch. Specifically, a revision in the electronics interface was necessary to prevent a data loss which had occurred on the first flight. The redesign of this interface as well as modifications made to the MUSTANG ground support equipment to support the upcoming launch is the subject of this thesis.

Chapter II documents the operational characteristics of the MUSTANG instrument itself, as well as the telemetry and support equipment provided by NASA as part of the sounding rocket experiment.

Chapter III investigates and identifies problems with the electronic interface package from the first sounding rocket launch. Areas where changes are necessary or new modifications are desired are identified.

Chapter IV provides an in-depth development of the design of the revised electronic interface package.

Chapter V documents the operation of all of the MUSTANG ground support equipment (GSE). This includes the Macintosh II computer, data acquisition boards, electronic interfaces, and all necessary software. This chapter serves as a reference for operation of the MUSTANG GSE, and documents improvements made to the equipment as a result of this thesis.

Chapter VI discusses the design and manufacture of the flight components of the electronic interface including the printed circuit boards and the flight box enclosure for the circuit.

Chapter VII presents all testing done on the interface circuit to validate its proper operation prior to flight.

Chapter VIII presents conclusions and recommendations for future projects associated with the MUSTANG instrument in the field of Electrical Engineering.

II. MUSTANG PAYLOAD AND SOUNDING ROCKET COMPONENTS

The MUSTANG and HIRAAS instruments are launched on a NASA Terrrier Black Brant sounding rocket. The major sections of the sounding rocket are shown in Figure 2-1. The Experiment section is under vacuum at the time of launch, and a door on the aft bulkhead opens at altitude to allow the instruments to make their observations. The major components of the MUSTANG instrument and the sounding rocket data collection and support system are described in this chapter.

The entire MUSTANG instrument is physically located in the Experiment section of the sounding rocket. The instrument consists of a middle ultraviolet spectrograph, an ITT image intensifier, a Hamamatsu linear image sensor with associated electronics and an electronic interface circuit. The construction of the electronic interface circuit is the subject of this thesis and is described in detail in the following chapters. All other components of the MUSTANG instrument are described in the following sections of this chapter.

The sounding rocket data collection and support system consists of a Pulse Code Modulation (PCM) encoder, a transmitter and an electric power distribution system. The instrument power supply is located in the High Voltage (HV) section, and provides DC electric power to the rocket payload. The PCM encoder and transmitter are located in the telemetry (T/M) section of the rocket. All of these subsystems are described in this chapter.

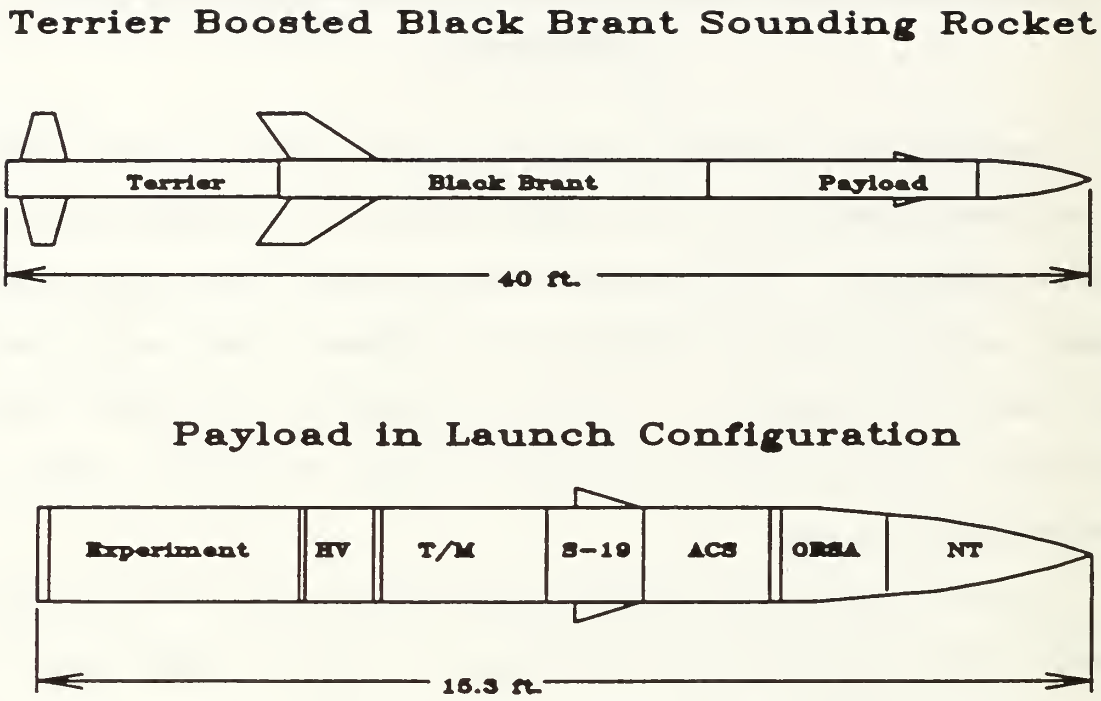

Terrier Boosted Black Brant Sounding Rocket
Terrier
Black Brant
Payload
40 ft.
Payload in Launch Configuration
Experiment
HV
T/M
S-19
ACS
ORSA
NT
15.3 ft.

Figure 2-1 Sounding Rocket Configuration Block Diagram

A. MUSTANG INSTRUMENT

The MUSTANG instrument consists of a 1/8th m off-axis telescope, a 1/8th m Ebert-Fastie spectrograph with a photo-detector system located at the exit focal plane and an electronic interface circuit. The optical equipment was designed at NPS and fabricated by Research Support Instruments, Inc. The interface circuit was designed and constructed at NPS as a result of this thesis. A mechanical drawing of the instrument is shown in Figure 2-2, and a photograph of the flight-ready MUSTANG payload is shown in Figure 2-3.

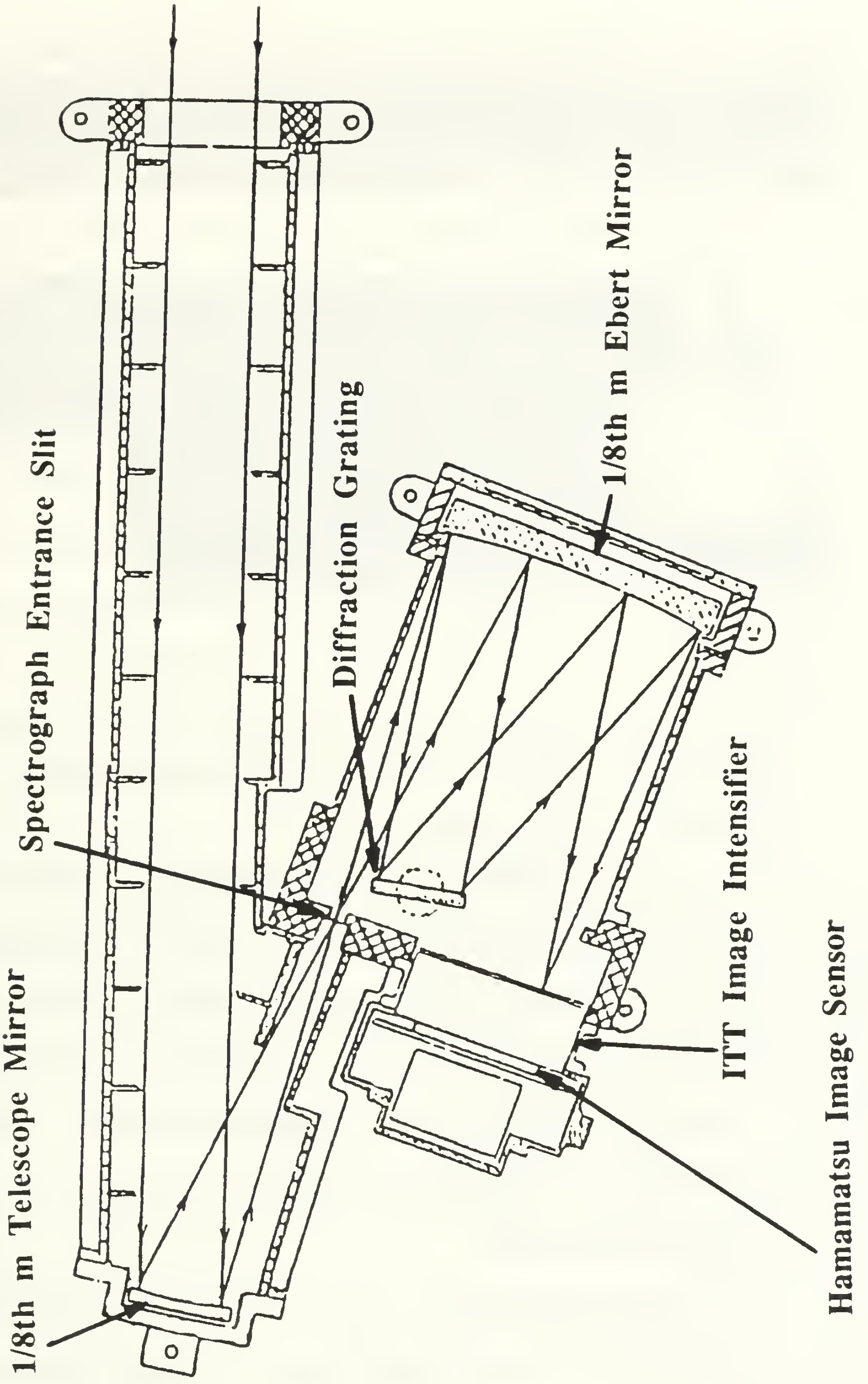


Figure 2-2 Mechanical Drawing of MUSTANG Instrument [After Ref. 3:p. 17]

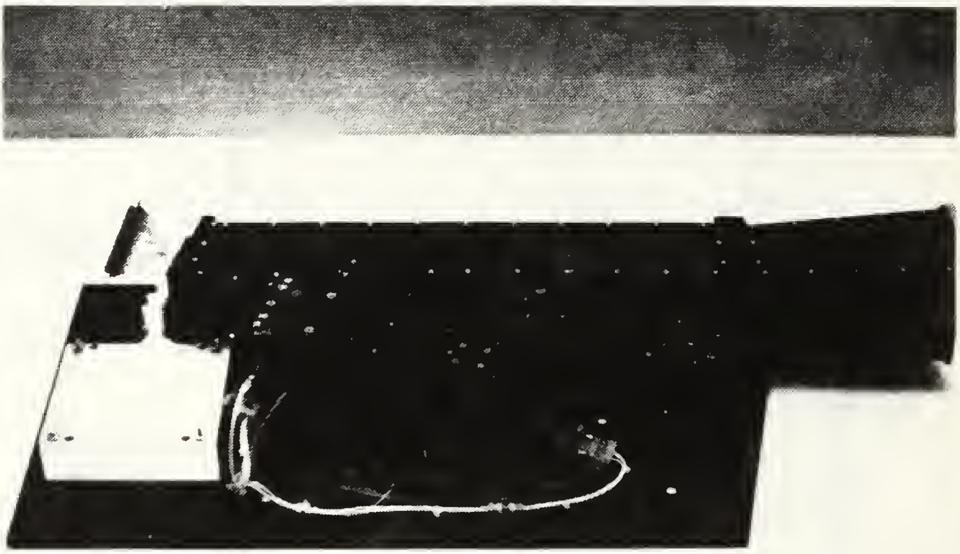


Figure 2-3 Flight-Qualified MUSTANG Payload

1. Ebert-Fastie Spectrograph

Ultraviolet light entering the telescope is collected by a 1/8th m spherical mirror. The mirror focuses the light onto a 5mm by 140µm vertical entrance slit. The Ebert mirror collimates the light onto a reflective diffraction grating. The grating reflects the collimated light back to the Ebert mirror where it is then focused onto the image intensifier at the spectrograph focal plane. Light incident on the image intensifier has a bandwidth of 1800Å to 3400Å [Ref. 3:p. 18].

2. ITT Image Intensifier

The image intensifier is an ITT F4145 Proximity Focused Channel Intensifier Tube with Dual Microchannel Plates. Technical Data for the ITT device is included in Appendix M. It consists of a quartz input window, a cesium telluride (CsTe) photo-cathode, two microchannel plates (MCP) in cascade, an aluminum screen coated with phosphor, and a fiber optic output window. The purpose of this device is to convert the incoming ultraviolet (UV) photons to visible photons so that they can be detected by the image sensor. UV Photons at the exit focal plane of the spectrograph strike the photo-cathode which cause photo-electrons to be generated. These electrons are accelerated down the MCP by an accelerating voltage. An electron avalanche occurs resulting in approximately 15,000 electrons produced for every one entering the MCP. An additional accelerating voltage accelerates the electrons to the phosphor screen where visible photons are produced [Ref. 3:p. 19]. The accelerating voltage across the MCP and the phosphor screen determines the gain of the MUSTANG instrument. It is produced by a high voltage power supply using a control voltage generated in the interface circuit. Technical data on the high voltage power supply is included in Appendix C.

B. HAMAMATSU LINEAR IMAGE SENSOR

The Hamamatsu S2300-512F Plasma-Coupled Device (PCD) Linear Image Sensor is a monolithic self-scanning photodiode array. Technical Data for this device is included in Appendix A. The photodiodes are highly sensitive to light in the 4000Å to 10000Å wavelength region as depicted in Figure 3 of Appendix A. Photons emitted from the image intensifier phosphor screen have a distribution in wavelength from 4750Å to 6000Å, and are sensed by the PCD image sensor [Ref. 4:p. 32]. The output window of the image intensifier and the PCD image sensor window are both made of fiber optic material. The two devices are placed physically in contact with each other in the MUSTANG instrument. With this arrangement, the UV spectrum in the 1800Å to 3400Å wavelength region can be observed by the MUSTANG instrument.

The monolithic PCD linear image sensor can be broken down into three basic parts: a 25mm by 5mm photosensitive area, a PCD shift register transfer section, and an output section. The operation of the device is described in the following sections of this chapter. Figure 1 of Appendix A is a block diagram of the device.

1. Light-Sensitive Section

This section consists of 512 p-n junction photodiodes arranged in linear array with spacing characteristics depicted in Figure 2 of Appendix A. The photodiodes are 36μm wide and 5mm tall. There is a spacing of 14μm between adjacent photodiodes which corresponds to a 50μm spacing between the centers of adjacent photodiodes. They perform two functions. First, they convert the optical energy of the incident photons into electrical energy. Second, they store this electrical energy in the form of charge stored in a capacitor. The photodiodes are manufactured to have a high sensitivity to photons of visible wavelength, and a low dark current. The dark current is caused by charge accumulated in the photodiodes when not exposed to any light. The dark current is a linear function of temperature, doubling with every 7°C rise in temperature [Ref. 5].

2. PCD Shift Register Transfer Section

This section of the detector provides the means for successively reading out the charge stored on each of the photodiodes. Hooked conductance transistors (HCDTs) make up the digital shift register. They are arranged in a linear fashion on the silicon substrate. When the proper phase clocking pulses are provided to the shift register, the HCDTs provide a negative address pulse which ripples down the array of switching transistors shown in Figure 1 of

Appendix A. The shift register uses the semiconductor plasma that is generated and destroyed in the silicon substrate as a result of carrier accumulation. Proper phasing of input clock pulses allows this plasma to transfer the state of the shift register down the array of 512 HCDTs. This plasma coupling transfer principle has a very slim operating margin; therefore, the Hamamatsu Driver/Amplifier circuit is utilized to generate the proper phasing signals. Reference 5 provides a more detailed description of the operating principles employed in the plasma-coupled device linear image sensor. The driver/amplifier circuit is described in more detail in a following section.

3. Output Section

This section applies the address pulses generated by the shift register to each photodiode in succession. This allows the charge on each photodiode to be read out in series. A bank of 512 bipolar pnp switching transistors is used for this purpose. When the negative address pulse is applied to the base of a particular switching transistor, the transistor turns on and couples the charge stored on its associated photodiode to the common output line. Reference 5 refers to this common output line as the video signal line.

C. HAMAMATSU DRIVER/AMPLIFIER CIRCUIT

The C2325 series low-noise driver/amplifier circuit was developed by Hamamatsu specifically for use with the PCD linear image sensors. The circuit generates the start pulse for beginning the scan of the detector. It generates the proper three-phase clock to drive the PCD and it contains the charge amplifier used to process the video signal in the integration mode. The driver/amplifier board consists of three basic parts. The controller section generates all necessary control signals. The driver section scans the PCD image sensor. The amplifier section processes the video data signal [Ref. 5]. Technical data for the driver/amplifier circuit is given in Appendix B. The circuit diagram is in Figure 4 of Appendix B.

1. Controller Section

The controller section receives two input signals from the MUSTANG interface circuit. One is a system clock which is the same as the Bit Clock received from the PCM encoder. The other is the positive Start signal which indicates the time for the start of a new scan of the image sensor. The controller passes these two signals to the driver section, and generates two output signals of its own. One output is the Trigger signal which indicates when the Video Data signal for each photodiode is valid. The Trigger signal is high for one period of the input Bit Clock indicating that the analog voltage is valid. It is low for the next three periods of the Bit Clock while the next photodiode is read out. A summary of the signals that are either used by, or supplied from the driver/amplifier circuit is given is Figure 2-4. An End of Scan, BEOS, signal is also generated by the controller, and it indicates that the last photodiode in the array has been read. This signal is not used in the MUSTANG application.

The frequency of the Bit Clock determines the rate at which the photodiodes are read out. A new one is read out every four periods of the bit clock. The frequency of the Start signal determines how long charge is allowed to accumulate in the photodiodes. After each photodiode is read out, the video signal is reset to ground. The photodiode begins to accumulate charge again until it is scanned in the next cycle. The time between reading the photodiode in one data frame to reading the same photodiode in the next frame is the same as the Start signal period [Ref. 5:p. 5].

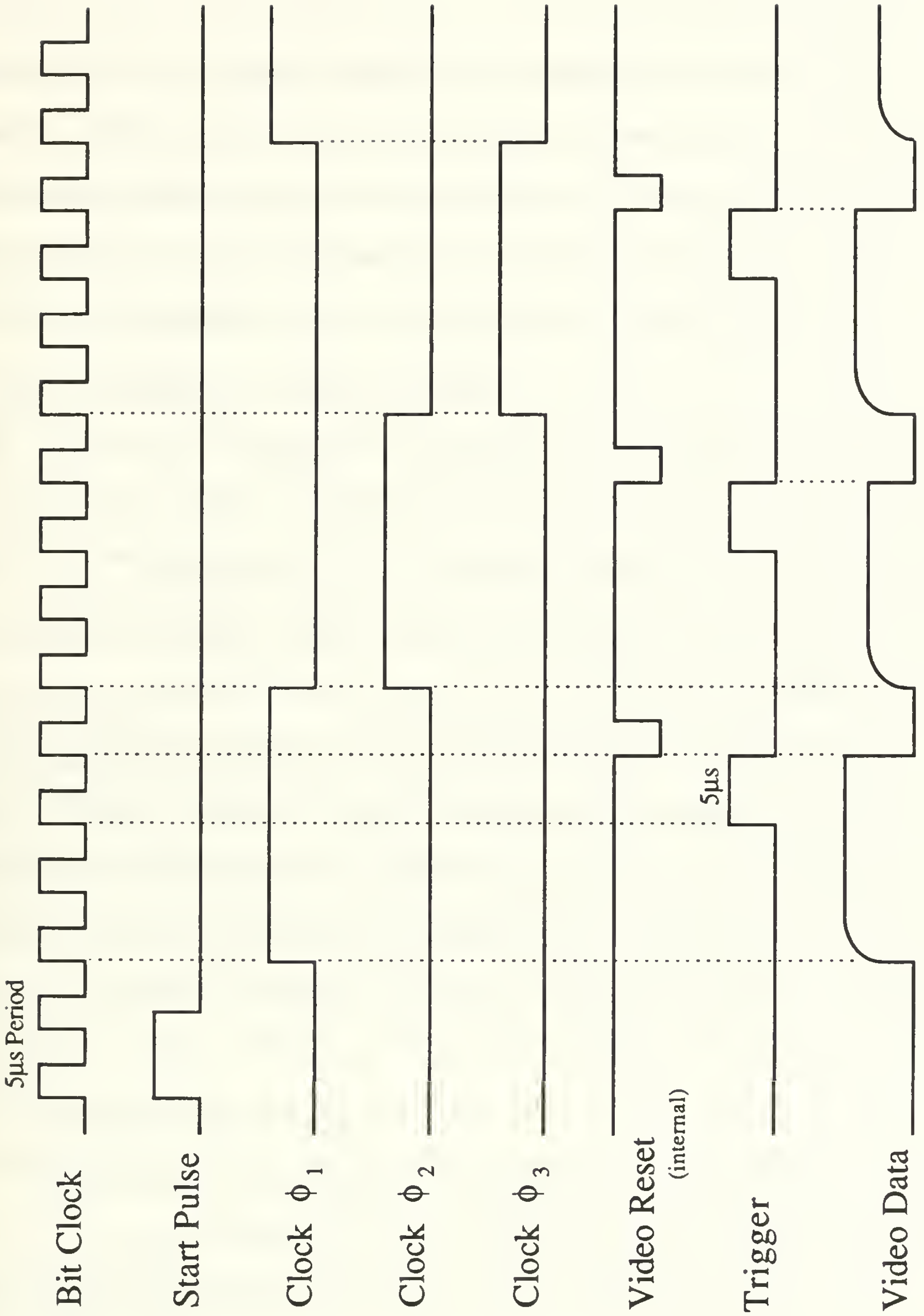


Figure 2-4 Driver/Amplifier Circuit Control Signals [After Ref. 5: p. 13]

2. Driver Section

The driver section receives the Bit Clock and positive Start pulse from the controller. It generates the proper three-phase clock. It also generates a negative Start pulse which is properly synchronized to the three-phase clock in order to begin the scan. The amplitude and the phase relationship of each phase of the three-phase clock are vital to the proper operation of the PCD shift register. These parameters must fall within a specific operating margin in order for the HCDT array to be able to pass the active state from one to the next adjacent HCDT. The Hamamatsu driver/amplifier board is matched to the appropriate PCD linear image sensor, so the user need not worry about generation of the proper clock phases and start sequence [Ref. 5:p. 2].

3. Amplifier Section

The amplifier section processes the video signal produced by the PCD image sensor integrated circuit. The processed video signal is referred to as the Video Data signal. Two methods are available to process the raw charge signal read out of the photodiode. The current-detection method uses a resistive load, but is nonlinear and suffers from a time skew problem; therefore, it is not used. The current-integration method uses a charge amplifier, and is utilized in the driver/amplifier circuit. The total current from the photodiode is fed to an operational amplifier in an integrator configuration. This integrated current signal has excellent linearity, even for very low-level outputs.

Most of the photodiode charge is read out in the first several hundred nanoseconds, so the Video Data signal has a rectangular shape with a rounded rising edge. This produces an analog signal that is stable for most of the 20μs period. The Trigger output signal is enabled when the Video Data signal is at its most stable point. The Trigger signal is used by the interface circuit to start analog-to-digital conversion as described in Chapter IV. The amplifier section applies a reset pulse to the Video Data signal to discharge it to ground following the falling edge of the trigger signal. This allows the next photodiode to be read out accurately. It also fully discharges the current photodiode so that it may again begin accumulating charge for the next readout cycle [Ref. 5:p. 5].

D. PCM ENCODER COMPONENTS

The Aydin Vector MMP-600 Series Pulse Code Modulation (PCM) encoder performs two basic functions. It provides all necessary clock synchronization signals to the experiments, and it collects any analog or digital data to be transmitted to the ground station during the sounding rocket flight. The PCM encoder for a particular sounding rocket mission is formed from a library of separate standard modules. The library is maintained at NASA Wallops Flight Facility in Wallops Island, Virginia. The modules are bolted together into what is known as the PCM stack. Only the PCM encoder modules which are pertinent to experiment data collection from the MUSTANG payload will be discussed in the following sections. For a full explanation of all available PCM modules, see Reference 6.

1. PX-628 Power Supply

The PX-628 Power Supply module is placed at one end of the stack. It serves two purposes. This module accepts +28V power from the rocket electrical distribution system and converts it to all DC voltages necessary to power the different modules in the stack. It also provides the master system Bit Clock to the modules in the stack. The Bit Clock frequency is programmable via several input pins on this module. Available bit rates are 800, 400, 200, 100, 50, 25, 12.5 and 6.25 kilobits per second (kbps). The 200kbps bit rate is used on this sounding rocket flight.

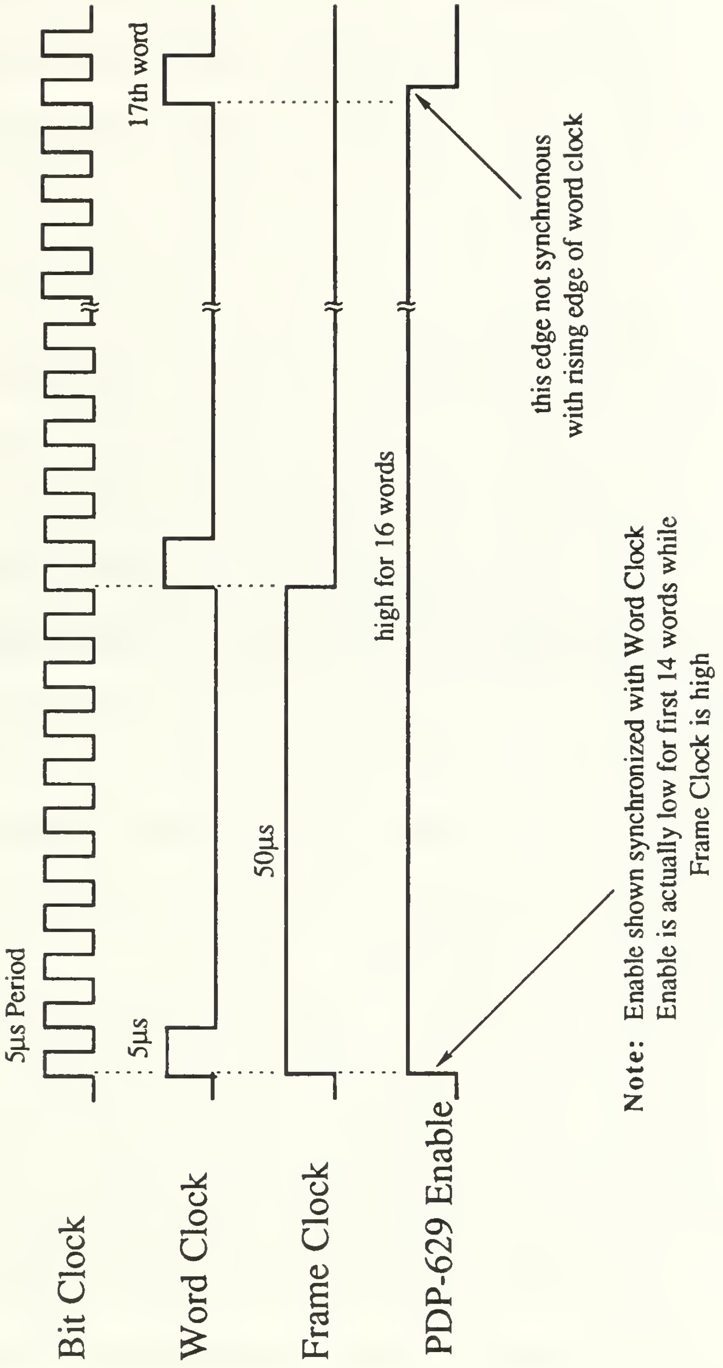
2. PR-614 Processor

The PR-614 Processor module contains the control circuitry for the entire PCM stack. The module executes the software program stored in the erasable programmable read-only memory (EPROM) in the end plate module. It controls the synchronization, timing and operation of the entire sounding rocket system.

3. TM-615P Timer

The TM-615P Timer module performs two major functions. The first function is to produce the Word Clock and Frame Clock from the system Bit Clock. Eight, nine or ten-bit words are programmable in the timer module. Ten-bit data words are used for this sounding rocket flight. The Word Clock signal provides a pulse every ten cycles of the Bit Clock. The structure of the data frame is also controlled by the EPROM software program. The Frame Clock provides a single positive pulse at the beginning of each new frame of data. All of the clock synchronization signals produced by the timer module are shown in Figure 2-5.

The second function of the timer module is to serialize the ten-bit digital data words prior to sending them to the transmitter. Digital data can enter the timer module from two sources. Data can come from an analog-to-digital converter module in the PCM stack. Data can also come from the digital multiplexer module discussed in the following section. The data words are serialized by use of the Word Clock and Bit Clock. The bit stream is then converted to a format compatible with the modulator and transmitter. Return-



Note: Enable shown synchronized with Word Clock
Enable is actually low for first 14 words while
Frame Clock is high

Figure 2-5 PCM Encoder Clock Synchronization Signals

to-zero, nonreturn-to-zero and bipolar data types are programmable in the timer module. The properly formatted data bit stream is then sent to the sounding rocket modulator and transmitted via an RF downlink to the ground station.

Binary digital data is transmitted to the ground station in structured frames. Each frame is separated in the PCM encoder by use of the Frame Clock. A frame of data corresponds to 1024 ten-bit words. 512 words in the frame are for the MUSTANG experimental data. The remaining 512 words are synchronizing words and Housekeeping data from various rocket systems. Format of the PCM communication frame is shown in Figure 2-6. The first 14 data words in the frame correspond to Housekeeping data. The next 16 words are the first 16 pixels in the MUSTANG spectrum. This cycle continues to the end of the frame as indicated in Figure 2-6. Several of the Housekeeping words in the PCM communication matrix are of particular concern to the MUSTANG instrument. They indicate when normal and high voltage power are applied to the instrument, and whether low or high gain is selected. These data words can be stripped out of the PCM matrix and monitored during rocket flight to determine the status of the MUSTANG instrument. The Housekeeping words of interest to the MUSTANG are indicated in Figure 2-6.

4. PD-629 30-Input Parallel Digital Data Multiplexer

The PD-629 digital multiplexer collects digital data from the MUSTANG payload in the form of parallel ten-bit words. It sends an Enable signal to the MUSTANG at the appropriate time in the PCM communication frame shown in Figure 2-6. The Enable signal tells the MUSTANG that the PCM encoder is ready to accept its data. The relationship of the Enable signal to the synchronizing clock signals is shown in Figure 2-5. The Enable signal is

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
2															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
3															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
4															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
5															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
6															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
7															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
8															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
9															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
10															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
11															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
12		1													●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
13															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
14															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
15		2													●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
16		3													●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
17															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
18															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
19		4													●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
20															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
21															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
22		5													●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
23		6													●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
24		7													●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
25															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
26															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
27															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
28															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
29															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
30															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
31															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		
32															●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		

MUSTANG Analog Signals:

1	Experiment High Voltage
2	± 15v DC/DC Monitor
3	5v DC/DC Monitor
4	28v Battery Monitor
5	5v Amplifier Monitor
6	15v Amplifier Monitor
7	5v High Voltage Monitor

● Indicates MUSTANG Experiment Data

10 bits/word
16 words/subframe
16 subframes/frame
1024 words/frame

Figure 2-6 PCM Communication Frame Matrix [After Ref. 4:p. 16]

high for 16 cycles of the Word Clock to collect 16 data words from MUSTANG, and then it goes low for 16 cycles to collect data from elsewhere in the rocket. The discrepancy with the falling edge of this Enable signal is discussed in detail in Chapter III. The method in which this module collects the data from MUSTANG is fully discussed in Chapter IV.

5. EP-612 End Plate

The EP-612 End Plate module attaches to the PCM stack at the end opposite to the power supply module. It contains the 256 by 8-bit EPROM which has been loaded with the software program to control the PCM encoder for the particular mission. A new EPROM is programmed for each specific sounding rocket flight.

E. ROCKET POWER DISTRIBUTION

Power is supplied to the Experiment section of the rocket from a +28V battery located in the T/M section. The rocket switches to internal battery power approximately 30 seconds prior to lift off. The battery is capable of supplying the necessary power for the rocket payloads for the entire flight duration. The rocket supplies two separate +28V power lines to the MUSTANG instrument. A timer in the T/M section controls when these power lines become energized. One +28V line supplies normal power to the MUSTANG instrument, and the other line supplies power to the high voltage circuitry. Each +28V supply is converted to +15V, -15V and +5V with two DC-to-DC converters located in the HV section of the rocket (see Figure 2-2).

The ±15V and +5V are distributed to the proper portions of the MUSTANG payload through a relay board which is also located in the HV section of the rocket. T/M timers are programmed so that instrument power is applied 85 seconds and high voltage power 96 seconds after the rocket launch.

III. PROBLEMS FROM PREVIOUS TEST FLIGHT

MUSTANG was launched on a sounding rocket from White Sands Missile Range in March 1990, on NASA flight number 36.053DE. The measurements of ultraviolet emissions in the earth's ionosphere recovered by the MUSTANG instrument as a result of this flight are the best data that the scientific community has seen to date in the 1800-3400Å wavelength region. Despite the success of the mission, there were some problems with data dropouts. Several Naval Postgraduate School theses have analyzed these data. The cause of the data loss was believed to be in the design of the electronic interface circuit. This belief was confirmed as a result of tests conducted on the electronic interface. These test results are reported in Chapter VI. The primary goal of this thesis is to redesign the electronic interface circuit so that it will provide the most reliable data possible from the 1800-3400Å wavelength region of the ultraviolet spectrum. To design a better interface, a full understanding of the problems and limitations of the existing electronic interface was necessary.

A. LEAST SIGNIFICANT BIT OF THE DATA WAS NOT USED

The least significant bit (LSB) of data was not used in the last flight, although it was digitized by the Analog-to-Digital (A/D) converter. Figure 3-3 of Reference 4 shows that the LSB had been grounded in the interface circuit. This was primarily due to the circuit components which had to be acquired in a relatively short time, prior to the rocket flight. A 12-bit A/D converter was the most readily available device that could perform the data conversion in the required amount of time. A single nine-bit First-in-First-out (FIFO) memory chip was used for memory storage. The Aydin Vector MMP-600 PCM Encoder was configured to accept ten-bit words from the MUSTANG payload. This meant that the last two bits of the digital word produced by the A/D converter had to be truncated. The availability of only a single nine-bit FIFO memory device meant that an additional bit had to be truncated. As a result, the tenth bit was discarded, and is zero in the data words recovered from the last MUSTANG flight.

This was not necessarily a problem with the original interface circuit, but rather an unnecessary hardware-imposed limitation. It was a limitation in the resolution of the data caused by the electronic interface circuit, and not required by the PCM encoder provided by NASA. Since the standard FIFO memory chip size is nine bits or less, this limitation was corrected in the revised interface circuit by adding an additional FIFO chip in parallel. Another option considered was to replace the FIFO with a wider version that could handle ten bits. The next size larger than nine bits is an 18-bit FIFO which is currently under development, but not yet commercially available.

B. EVERY 17TH DATA WORD IN THE SPECTRUM WAS LOST

Analysis of the data from the last MUSTANG flight revealed that an apparent wavelength shift was present in the spectral components. The shift was more pronounced at the higher wavelength end of the spectrum than at the lower end. By comparing some known atmospheric emissions to the data, it was suspected that every 17th data word in the frame of 512 data words was skipped somehow. Inspection of the enable signal provided by the PD-629 30-input Bi-Level Multiplexer showed that it did not go low with the rising edge of the Word Clock for the 17th word of the subframe as expected. The PCM Encoder

Handbook is not specific on timing characteristics of the falling edge of the enable signal as shown in Figure 3-1.

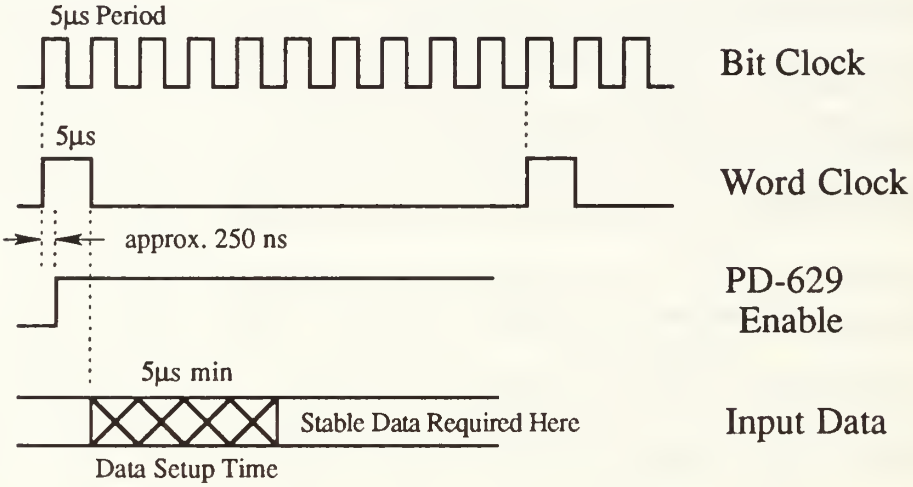


Figure 3-1 PD-629 Timing Diagram [After Ref. 6:p. 43]

The reason that every 17th word was discarded has to do with the way that the read enable pulse to the FIFO memory chip was formed. The Word Clock and Enable signals of Fig. 3-1 were supplied to the inputs of a nand gate and the output was used as the read enable pulse for the FIFO. Since the Enable signal was found to overlap the 17th word pulse as shown in Figure 2-1, a spurious read enable pulse was sent to the FIFO. This caused a word to be read out of memory when the PCM Encoder was not looking for a data word from the MUSTANG payload; therefore, the word was lost. This was clearly a design flaw of the original electronic interface circuit which could not have been discovered until after the launch.

Reference 6 does give some warning that the Enable signal provided by the PD-629 module is not a clean signal. It warns that decoding spikes may be present on the Enable lines, and gives a suggested circuit to create a gated enable signal. This gated enable signal in conjunction with the Word Clock should then be used to trigger the interface circuitry. This guidance was not followed in the original interface circuit, but was adhered to in the present circuit.

The main reason that this problem was not identified prior to launch has to do with the artificial testing environment set up in the laboratory. The Ground Support Equipment (GSE) used to test the MUSTANG in the lab will be described in detail in Chapter V. In short, the GSE provides all of the clocking signals which are normally provided by the Aydin Vector MMP-600 PCM Encoder on the rocket. These signals are perfectly synchronous, and the overlap in the Enable signal is not present in the GSE. Consequently, when the interface circuit was tested in the lab, it functioned normally with no lost data words. It was not until the circuit operated on the rocket with the imperfect Enable signal, that the data loss problem became apparent.

This problem was prevented in the revised electronic interface circuit by adhering to the guidance for constructing a gated enable signal in Reference 6 [Ref. 6:pp. 43-44]. In addition, we conducted a special test of the prototype interface circuit with the actual PCM Encoder hardware on the rocket prior to construction of the flight qualified circuit. This test is described in detail in Chapter VII.

C. ADDITIONAL THREE DATA WORDS LOST IN THE SPECTRUM

Further analysis of the data from the first MUSTANG flight revealed that the loss of every 17th data word in the spectrum did not fully account for the apparent wavelength shift observed in the spectrum [Ref. 3:p. 72]. The location of some spectral features suggested that an additional three data words had been lost. In Reference 3, LT Carl Anderson predicted that one of the additional lost data words occurred adjacent to one of the every-17th-words that was dropped out. This meant that two adjacent data words in the spectrum were lost. This prediction was based on a comparison between the observed and theoretical line profile for a known oxygen emission at 2972Å.

At the end of every frame of 512 data words in the MUSTANG flight data, were 32 data words that were zero, indicating that 32 words had been lost. This also supports the theory that an additional three data words were lost somewhere in the spectrum. The exact cause of this additional data loss has not been determined. The only plausible explanation for the loss is that spurious read enable pulses were created which caused the FIFO to skip three more words. This could be due to the noise spikes on the Enable line mentioned in Reference 6. If a noise spike occurred at the same time that the Word Clock was high, a spurious read enable pulse would be sent to the FIFO. If this pulse were of sufficient duration, 120ns, an additional data word would be lost.

The solution to the whole data loss problem hinged on creating a clean, synchronous Enable signal to use for data transfer. Using a gated enable signal as described in Reference 6 corrected the problem of the additional three data words being lost. This does not explain exactly how they were lost on the first MUSTANG flight, but it does correct the problem. The test described in Chapter VI verified this solution.

D. FIFO READ TIMING SPECIFICATIONS WERE VIOLATED

One of the fundamental design concepts in electronic circuit design is worst-case timing analysis. Propagation delay and setup-and-hold time specifications are given for all integrated circuits in their associated databooks. In analyzing the proper circuit operation, one must consider the worst-case values of these timing parameters in order to ensure the circuit will function as designed in all cases. Modern integrated circuits are very reliable and typically operate much better than their worst case specifications, but this should never be relied upon in circuit design.

The portion the the original interface circuit which read data out of the FIFO memory and latched the data did not stand up to worst-case timing analysis. Data read out of the FIFO only stays valid for a minimum of 5ns after the read enable pulse returns high. The original interface circuit used the same pulse for the read enable and the latch signal to the octal latches. The latch signal was derived by passing the read enable pulse through a nand gate so that the inverted pulse could be used. This also imposes a delay on the latch pulse which is delayed a maximum of 15ns from the read pulse. The high speed CMOS latches also had a data hold time requirement of a minimum of 12ns. This means that data must be valid at the input to the latch for at least 12ns after the latch pulse goes low. These timing parameters are demonstrated in Figure 3-2. In the worst-case conditions the data may have already become invalid even before the latch pulse went low. Under these conditions this would have resulted in the octal latches latching invalid data. The fact that the circuit appeared to function correctly in this application is a tribute to modern integrated circuits, and shows that they functioned much better than their worst-case performance. This kind of circuit design is best avoided. The issue of timing analysis was treated very meticulously in the design of the revised interface circuit, and is related in Chapter IV.

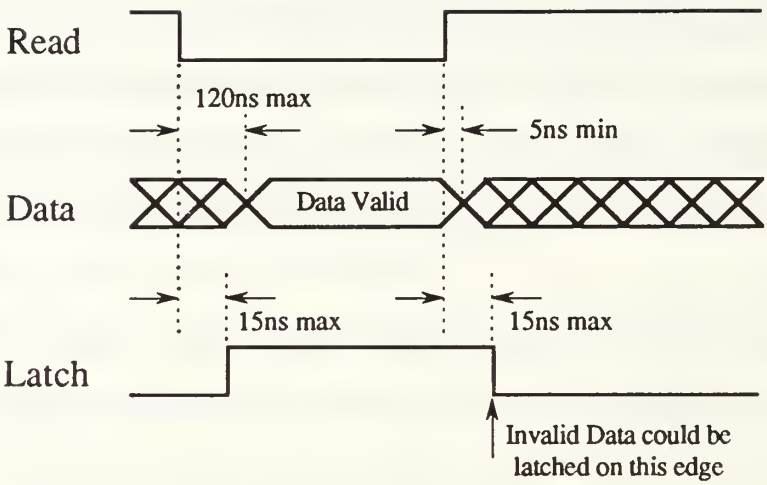


Figure 3-2 Worst-Case Read Timing Analysis

E. FIXED INSTRUMENT GAIN FOR ENTIRE FLIGHT

Because it operates between the altitudes of approximately 100 to 320km, the MUSTANG instrument sees a variation of three orders of magnitude in intensity. Selection of the instrument gain was a tradeoff between not saturating the detector at high intensities, and ensuring that useful data was still obtained at low intensities. The gain is set by the level of a control voltage applied to the high voltage power supply. The gain of the instrument is an exponential function of that control voltage. Consequently, the gain selection is a very important issue in the preparation of the MUSTANG instrument for flight.

The ability to change the instrument gain while it is in flight is a very desirable feature. This would allow data acquisition at low gain when the ultraviolet intensity is high and high gain when the intensity is low. This would provide a greater dynamic range in the actual data gathered from a single rocket launch. Since the instrument gain is an exponential function of the control voltage, the voltage would not have to change much to have a large effect on the gain. This implies that a simple circuit modification is all that is necessary, along with associated control signals, in order to make the instrument gain adjustable during flight.

The short time constraints and difficulty with the original electronic interface circuit prevented this feature from being added on the first MUSTANG flight. Redesigning the interface, and ample lead time allowed its inclusion in the revised interface circuit. The gain selection portion of the interface is discussed in detail in Chapter IV.

F. FLIGHT QUALIFIED PARTS NOT UTILIZED

An important consideration in any electronic circuit construction for a space or military application is that it utilize high reliability components. The military specification for high reliability integrated circuits is MILSTD 883 Class B. The integrated circuits which conform to this standard have been individually, rigorously tested to ensure reliable performance across a wide temperature range. It is highly desirable to use such components on a sounding rocket mission where much time, effort and money has gone into planning and execution of the flight. The time during which data is actually recorded in the flight is approximately eight minutes, so it is essential that the equipment be functioning properly or all data will be lost. Separate military specifications exist for radiation hard components, but that is not a concern in this application. The sounding rocket flight is relatively short, and the rocket only reaches a maximum altitude of approximately 320km where radiation exposure is not a great concern for a short time interval.

All MILSTD integrated circuits come with documents which attest to their conformance to the specifications, and provide a traceability record for the individual component. Although these components cost a great deal more than their commercial grade counterparts, it is money well spent in this application. Another factor to consider, is that MILSTD components can be harder to find, and typically have a longer lead time when ordering from a manufacturer or distributor. The short development time of the original MUSTANG interface circuit was the primary reason that MILSTD components could not be procured in time for launch. Enough time existed in the development of the revised interface circuit so that it will be flown with all MILSTD 883 Class B integrated circuits.

Another important circuit component which has a military specification is the D-Subminiature connector (D-Sub). High reliability D-sub connectors are made to conform to MILSTD 24308, and are available in several types. These are essential in the construction of flight qualified circuits. A connector can be the weakest link in an otherwise well-designed electronic circuit. Bad connectors are often times the hardest problem to diagnose in circuit troubleshooting. MILSTD D-sub connectors were used on the original interface circuit and will continue to be used in the revised circuit.

The problems and considerations presented in this chapter document the goals which had to be kept in mind in redesigning the electronic interface circuit. The design of the revised interface is the subject of the next chapter.

IV. ELECTRONIC INTERFACE CIRCUIT DESIGN

The purpose of this chapter is to describe in detail the method in which the MUSTANG electronic interface circuit was redesigned to provide more reliable data acquisition. Because of the problems with the original interface circuit outlined in the previous chapter, it was prudent to begin design from the basic elements of the flight configuration hardware. The MUSTANG instrument itself, as described in Chapter II, provides a series of analog voltages proportional to the intensity of various wavelengths in the ultraviolet spectrum. A clock signal and a starting synchronization pulse must be provided to the instrument. A new analog voltage is produced every 20µs and it is valid for only 5µs. The Aydin Vector MMP-600 PCM Encoder hardware in the rocket telemetry section provides the clock signals shown in Figure 2-5. It can be programmed to accept data from the MUSTANG payload that is analog or digital in the form of eight to ten-bit words. A new data word is accepted from the instrument every 50µs for 16 data words in a row. A period of time lapses where 16 data words are accepted from elsewhere in the rocket, and then 16 more words are accepted from the MUSTANG instrument . This cycle continues 32 times for a total of 1024 data words acquired by the telemetry section (512 MUSTANG words plus 512 Housekeeping words). A synchronizing frame pulse is then sent and the cycle repeats.

This asynchronous nature of data transfer from the MUSTANG payload to the rocket telemetry section presents a considerable design challenge. The electronic interface circuit must reliably transfer data from the MUSTANG to the rocket telemetry while adhering to the above listed specifications. The best way to perform this data transfer is described in the following sections.

A. SELECTION OF DATA ACQUISITION METHOD

Several alternatives were available for transferring the analog voltage produced by the MUSTANG instrument to the PCM encoder in the rocket telemetry section. One is to directly transfer the analog voltage signal to the PCM encoder. A second alternative is to sample and hold the analog signal at the interface circuit in order to perform an analog-to-digital (A/D) conversion. The digital word would then be transferred to the PCM encoder. The final alternative is to just perform a direct A/D conversion in the interface circuit, and transfer the digital word. The first two alternatives were ruled out for the reasons described below.

1. Direct Transfer of the Analog Voltage Signal

Since the PCM encoder can be programmed to accept analog data as an input, it is possible to transfer the analog signal directly. The PCM encoder then performs its own A/D conversion to form the digital words that are telemetered to the ground station. There are two separate reasons that make this method impractical. The physical distance that the analog signal must travel from the MUSTANG payload to the rocket telemetry section is on the order of five feet. This long signal path would introduce an unacceptable amount of noise and attenuation on the analog signal, resulting in unreliable data. Figure 2-1 illustrates the physical location of these components. Additionally, this method of data acquisition is physically impossible since the MUSTANG produces analog voltage signals at a constant rate and the PCM encoder acquires data in an asynchronous manner.

2. Sample and Hold for Analog-to-Digital Conversion

The analog signal from the MUSTANG could be fed to a sample and hold circuit in the electronic interface during the 5μs when the analog voltage is valid. In the remaining 15μs before the next analog voltage becomes valid, the signal could be digitized with an A/D converter. The digital data word could then be transferred to the PCM encoder much more reliably than an analog signal. Digital data is easily stored, so a memory device solves the asynchronous data transfer problem. The problem with this method is that the sample and hold circuit imposes an unnecessary level of complexity on the interface. The reliability of the interface circuit is the most important design factor, and the next alternative provides a more reliable method of data transfer.

3. Direct Analog-to-Digital Conversion

Direct A/D conversion of the analog signal at the interface circuit is the simplest method of transferring the data from the MUSTANG to the PCM encoder. This allows for digital data transfer from the instrument to telemetry which is preferred. A single component performs the conversion directly which contributes to high reliability. The only problem with this method is that the A/D conversion must occur very rapidly, as the analog signal is only valid for 5μs. This requires a relatively complex and expensive A/D converter. Even considering the cost, this is a more desirable alternative than the less reliable approach of using a sample and hold circuit.

B. DIGITIZING OF THE ANALOG SIGNAL

An Ultrafast Hybrid A/D converter was selected to perform the direct A/D conversion described in the above section. Technical data for the Analog Devices HAS-1202A A/D converter is located in Appendix D. This same integrated circuit was flown on the last MUSTANG flight and provided very reliable operation. It can perform a 12-bit conversion in a maximum of 1.56μs based on the minimum pulse width of the Encode command. The largest data word that the PCM encoder can accept is ten bits, so the last two bits from the A/D converter will be truncated. Several ten-bit A/D converters are available, but they do not meet the stringent conversion time requirements. The Analog Devices A/D converter is not available in a MILSTD 883 Class B screened version; however, a component which has been screened to all military temperature requirements and most MILSTD 883 requirements, is available and was procured for this mission.

1. Control Signals

Only one input control signal is required by the A/D converter, and it provides one control signal as an output. A positive Encode command pulse of minimum duration 50ns starts the A/D conversion process. Data conversion begins 60ns after the rising edge of the Encode command, and is signified by the rising edge of the Data Ready signal. If the Encode command pulse is longer than the required minimum, then data conversion takes a maximum of 1.46μs from the falling edge of the Encode command signal. If the Encode command is the minimum pulse width then data conversion is complete a maximum of 1.56μs after the rising edge of the Encode pulse. Completion of the data conversion is indicated by the falling edge of the Data Ready signal. See Figure 1 in Appendix D for a timing diagram of these signals.

As described in Chapter II the Trigger signal from the Hamamatsu Driver Amplifier circuit goes high when the output analog voltage from the MUSTANG instrument is stable. This rising edge is used to start the data conversion process in the A/D converter. The Trigger signal cannot be used directly since it remains high for the entire 5µs that the analog voltage is stable. A positive Encode signal pulse is created with a monostable multivibrator which is triggered by the rising edge of the Trigger signal. Technical data for the 54LS221, monostable multivibrator, is listed in Appendix I. The pulse width of the positive pulse produced by the monostable is programmable by selecting an external resistor and capacitor. The equation for the pulse width is shown in Equation 4-1.

$$t_w = R_{ext} C_{ext} \ln(2) \tag{4-1}$$

Good, quality components must be selected for the external resistor and capacitor since the duration of the produced pulse is critical to circuit operation. Metal film resistors with a 1% tolerance were selected for use with the monostable multivibrators in the interface circuit. Poly film capacitors with a 5% tolerance were also selected. Component values were selected to give an Encode signal pulse width of 525ns. This caused the data conversion to complete within a maximum of 1.985µs from the rising edge of Encode. This is fast enough to ensure the data conversion is complete prior to the noisy portion of the analog signal which happens at the Bit Clock transition, 2.5µs after the rising edge of Encode [Ref. 4:p. 74].

2. Gain Selection for Input Analog Voltage Range

The Analog Devices A/D converter allows analog input voltages in the range of zero to 10.496 volts. If the input voltage is expected to be less than the maximum allowed by the A/D converter, then the input voltage can be scaled by proper selection of an external resistor. The external scaling circuit is shown in

Figure 2 of Appendix D. The value of the external resistor, R2, is calculated from Equation 4-2, given the full scale input voltage.

$$R2 = 860\left[\frac{(V_{fs} \times 97.66) - 165}{1025 - (V_{fs} \times 97.66)}\right] \qquad (4\text{-}2)$$

The maximum analog voltage expected to be supplied by the MUSTANG instrument is 8.24V. This corresponds to a resistor value of 2500Ω for R2 which was used in the electronic interface.

C. MEMORY STORAGE REQUIREMENT

Once a data word is produced by the A/D converter, it must be temporarily stored in the interface circuit until the PCM encoder is ready to accept it. This is due to the asynchronous nature in which the PCM encoder acquires data from the MUSTANG payload. The Hamamatsu PCD Linear Image Sensor and Driver Amplifier circuit provide a new analog voltage signal corresponding to a particular ultraviolet wavelength every 20µs. This occurs synchronously until the entire linear image sensor array of 512 photodiodes is read out. The data is produced in a total of 512 × 20µs = 10.24ms. The PCM encoder acquires 16 data words at intervals of 50µs followed by 800µs with no data accepted from the MUSTANG payload. The entire array of 512 data words from the MUSTANG payload is acquired in a total of 512 × 50µs + 32 × 800µs = 51.2ms. See Figure 2-6 for construction of the PCM communication matrix.

The two differing data rates clearly indicate the need for some type of temporary data storage in the interface circuit. The memory device must support an asynchronous read and write capability since both operations must be allowed to proceed at their own rates. The memory device must be capable of storing ten-bit words. 512 data words are produced for each complete readout of the linear image sensor, so no more than 512 ten-bit words would need to be stored at any given time. The maximum data storage capacity works out to 384 data words after the image sensor is completely read out in 10.24ms. Two data storage alternatives are possible. A static random access memory (RAM) or a FIFO memory device would be suitable for this application.

1. Static RAM Storage Device

Very fast access static RAM devices are available for use in this application. Configuring existing static RAM integrated circuits to store a maximum of 384 ten-bit words would not be difficult. The difficult aspect of this alternative would be in the extra supporting hardware required to address the RAM. Some external counters or registers would be required to keep track of data addresses within the RAM. This would add complexity, as well as cost and circuit board area to the interface circuit design. For these reasons, a RAM storage device was ruled out.

2. FIFO Memory Storage Device

The FIFO memory device is the simplest and most compact alternative for temporary data storage in the interface circuit. All addressing logic is internal to the device, and it can handle asynchronous reads and writes by simply applying the appropriate control signals. The only difficulty with this alternative is that the largest FIFO's available are only nine bits wide. Several 18-bit FIFO's are under development, but are not yet commercially available. To accommodate the ten-bit words in this application, two FIFO devices would have to be connected in parallel. FIFO devices that store 4 and 5-bit words are currently available; however, they do not store as many data words as the larger ones. The simplest alternative was to connect two identical nine-bit FIFO's in parallel which resulted in eight of the 18 bits not being utilized. Although this may seem wasteful at first glance, it consumed less circuit board area and power than other FIFO configurations using ten-bit data words. The ideal solution would be to use an 18-bit FIFO when it becomes available so that memory storage can be accommodated with a single integrated circuit.

The device selected for use in the interface circuit is the same single FIFO that was utilized in the original interface circuit, the IDT 7201 CMOS Parallel First-In-First-Out FIFO manufactured by Integrated Device Technology, Inc. Technical data on the IDT 7201 is included in Appendix F. The device has the capacity to store 512 nine-bit data words. Parallel connection of the two devices to accommodate ten-bit words was performed by simply connecting several of the control signals together. Figure 13 of Appendix F shows two devices connected in the width-expansion mode. Common Reset, Read and Write command signals are connected to both devices, allowing them to function as one unit. The Expansion In, XI, input is grounded since the depth expansion capability is not necessary. The First Load/Retransmit, FL/RT, input is tied to +5V since there is no provision for retransmission of data in the PCM encoder circuitry. The Full Flag, Half-Full Flag and Empty Flags are not used in this application. Further discussion of the command signals is included in the following sections.

D. FRAME SYNCHRONIZATION OF DATA ACQUISITION

The 512 MUSTANG data words in the communication matrix correspond one-to-one with the 512 photodiodes in the linear image sensor. A method had to be devised to ensure that the first MUSTANG data word in the frame corresponded to the first photodiode read out in the linear image sensor array for each successive data frame. This meant that both the image sensor and the FIFO memory must be reset at the start of each communication frame. This was simple to do, since a Frame Clock pulse is provided by the PCM encoder at the start of each successive frame of data. The pulse is 50μs long, which is the period of the Word Clock (see Figure 2-5).

The Hamamatsu driver amplifier circuit requires a positive Start pulse of 500ns minimum duration to initiate its scan of the linear image sensor. That is the only requirement to initiate a new scan on the image sensor. The FIFO memory device requires a negative Reset pulse of 120ns minimum duration to reset the read and write pointers within the device. The timing diagram for the FIFO reset is given as Figure 2 of Appendix F. This timing diagram requires that the Read and Write command signals remain high for a minimum of 120ns prior to the Reset signal returning high. The first write to the FIFO cannot occur for a minimum of 20ns after the rising edge of the Reset signal.

The above restrictions are easily met if the Reset and Start signals are the inverse of each other. They did not need to be as long in duration as the Frame Clock pulse, so another monostable multivibrator was used to generate the pulses triggered from the rising edge of the Frame Clock pulse. Circuit elements were selected to create a pulse of 6.5μs duration from Equation 4-1. The monostable, of Appendix I provides complemented outputs so both Reset and Start signals were created from a single monostable. The only timing difference in these signals results from the differing propagation delays of the monostable on a low-to-high transition when compared to a high-to-low transition. This is illustrated in Figure 4-1.

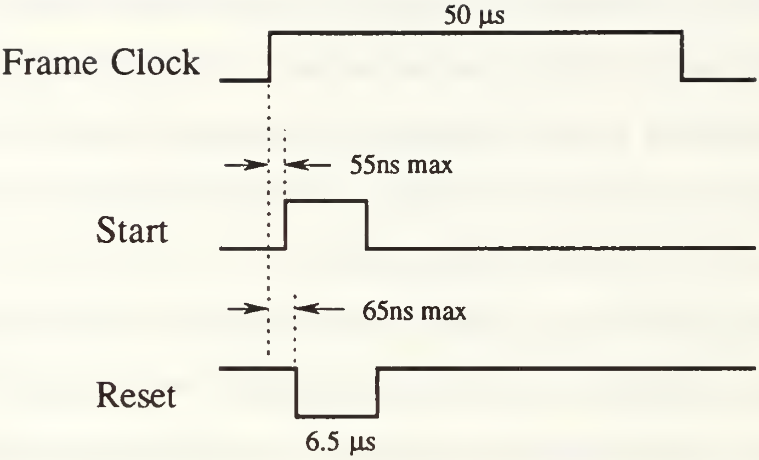


Figure 4-1 Frame Synchronization Signals

A read operation is guaranteed not to occur within the restricted time interval of reset, since the PCM encoder does not assert the Enable signal for the first 14 words of the PCM communication matrix. A write operation is guaranteed not to occur within the restricted time interval of reset, since the first Trigger pulse is not asserted until 9.8µs after the falling edge of the Start pulse. This is shown in Figure 3 of Appendix B. The Read and Write command signals are discussed in the following sections.

E. FIFO WRITE CYCLE TIMING REQUIREMENTS

The relationship of all necessary timing signals for the data write cycle is shown in Figure 4-2. A given analog voltage signal from the MUSTANG instrument is stable for 5µs while the Trigger signal is high. The signal is digitized by the A/D converter in the first 1.985µs. This leaves approximately 3µs to get the data word written into the FIFO memory before the signal becomes invalid. The falling edge of the Data Ready signal from the A/D converter signifies that conversion is complete and the digital data word is valid.

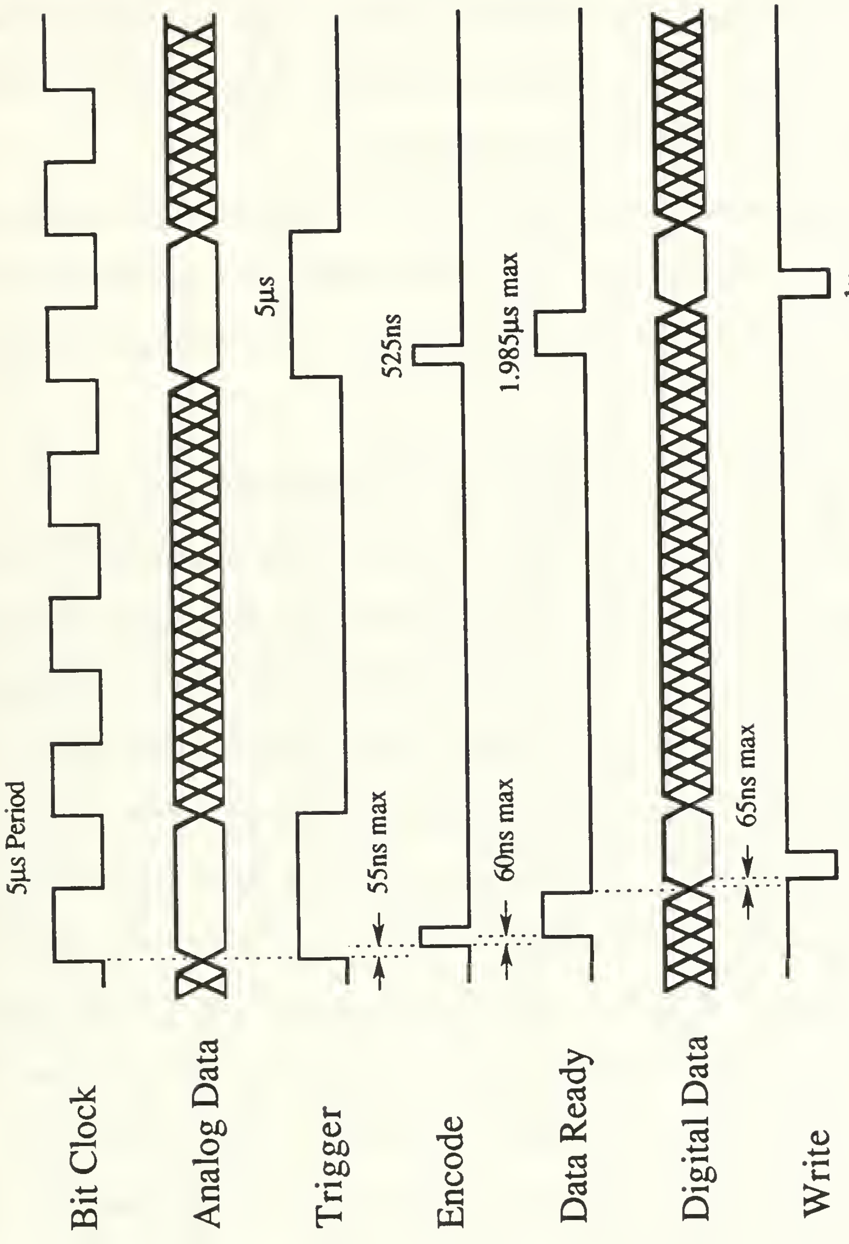


Figure 4-2 Write Cycle Timing Diagram

The data word stays valid until the next Encode pulse goes high. The write cycle timing requirements for the FIFO are given in Figure 3 of Appendix F. The minimum Write signal pulse length is 120ns. Digital data to be written into the FIFO must be setup for a minimum of 40ns before, and held for a minimum of 10ns after the rising edge of the Write pulse.

A Write command pulse length of 1μs was a good compromise which met all of the above requirements. The Write signal was generated with a third monostable multivibrator utilizing Equation 4-1 to compute external circuit component values.

F. FIFO READ CYCLE TIMING REQUIREMENTS

The read cycle timing design is the most critical portion of the interface circuit design. This portion of the circuit was the source of the data loss problems experienced on the original MUSTANG flight. Figure 4-3 is a comprehensive summary of all of the control signals which play a part in the read cycle timing. The read cycle timing requirements for the FIFO are given in Figure 3 of Appendix F. The minimum duration Read signal pulse is 120ns. Data becomes valid out of the FIFO a maximum of 120ns after the falling edge of the Read signal. Data out of the FIFO remains valid for a minimum of 5ns after the rising edge of the Read signal. Data is to be read out of the FIFO only when the PCM encoder is ready to receive a new data word from the MUSTANG payload. As shown in Figure 3-1, the PCM encoder asserts its enable signal, and then latches digital data from the MUSTANG a minimum of 5μs after the falling edge of the Word Clock. All control signals generated in the interface circuit hinge around setting up stable data out of the FIFO to support this timing requirement.

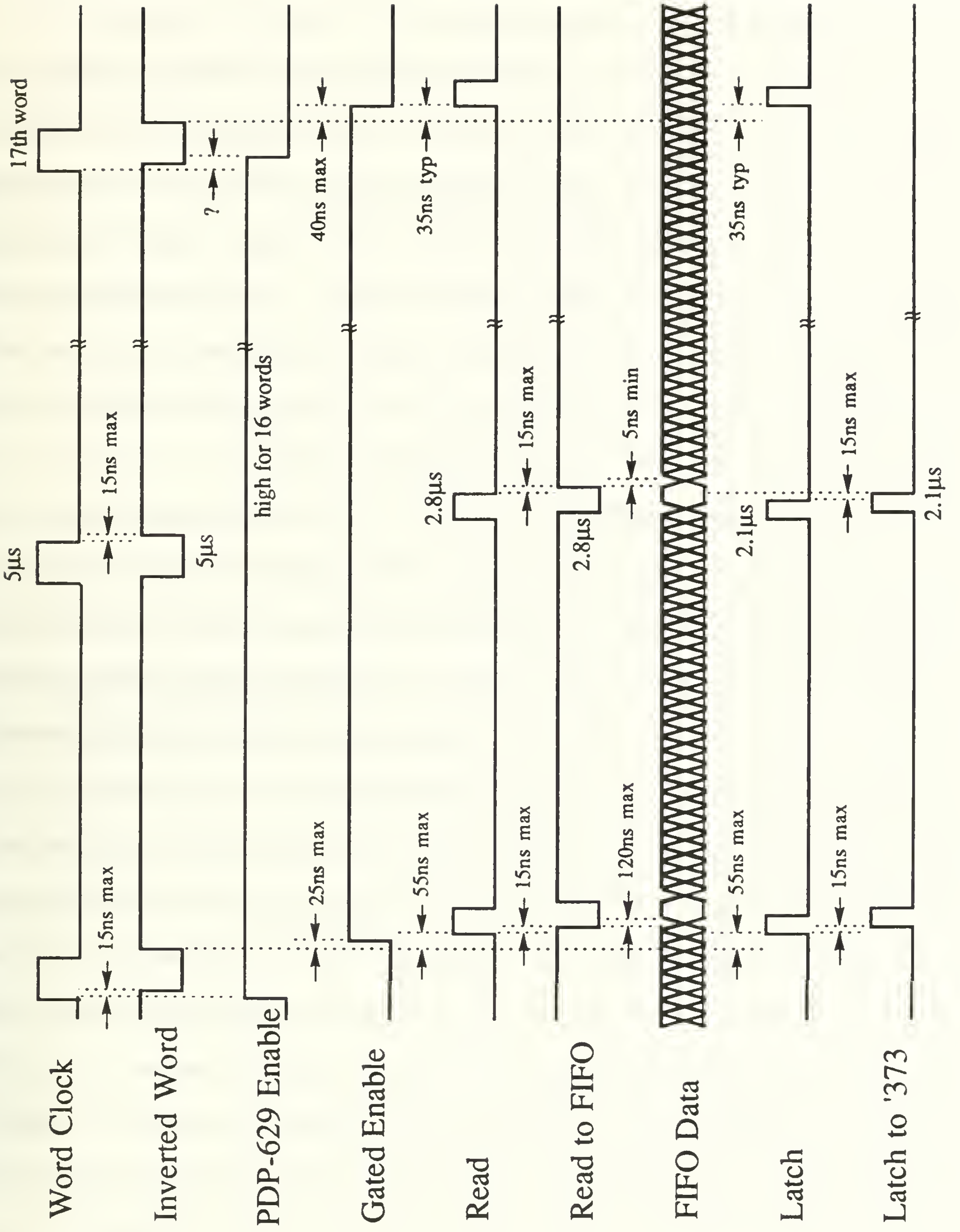


Figure 4-3 Comprehensive Read Cycle Timing Diagram

1. Creating a Clean Enable Signal

The Enable signal from the PDP-629 module is designed to signal the payload when the PCM encoder is ready to receive data from the instrument. The problem experienced in the last flight was that the Enable signal did not go low prior to the rising edge of the 17th Word Clock pulse. This is depicted in Figure 4-3 as an unknown overlap in the two signals. Since the Read signal in the original interface circuit was formed by simply nanding the Word Clock with the PDP-629 Enable signal, a spurious Read pulse was generated which read out and lost an additional word in each communication subframe.

Based on recommendations in Reference 6, a gated Enable signal was formed from the PDP-629 Enable signal. The purpose for this was twofold. The gated Enable signal would be synchronous in relation to the Word Clock and it would be free from noise spikes. The recommended circuit of Figure 22 in Reference 6 was utilized. The Word Clock was provided to both inputs of a positive nand gate which produced an inverted Word Clock at the output, delayed by a maximum of 15ns. The inverted Word Clock was used as the clock input to a positive-edge-triggered D-type flip-flop. Technical data for the flip-flop and nand gate is included in Appendix J and Appendix K, respectively. The data input to the flip-flop was the PDP-629 Enable signal. This meant that the Enable signal was latched into the flip-flop on the falling edge of the actual Word Clock. Note that the Enable signal is low before the falling edge of the Word Clock for the 17th word. This created the synchronous gated Enable signal shown in Figure 4-3.

2. Creating a Reliable Read Signal

Now that a reliable Enable signal has been formed, a Read signal must be created to get the data out of the FIFO in time for the PCM encoder to read it. The Word Clock can no longer simply be nanded with the gated Enable signal since the first data word would be missed. The gated Enable signal, in essence, follows the Word Clock. A new Read pulse had to be generated, and this was done with a monostable multivibrator. The positive Read signal shown in Figure 4-3 was generated by triggering a monostable with the rising edge of the inverted Word Clock. The pulse duration was selected to be 2.8μs by choosing circuit components to satisfy Equation 4-1. This pulse length would ensure that data would be valid out of the FIFO in time for the PCM encoder to read it. The FIFO requires an active-low Read signal so the generated Read pulses were nanded with the gated Enable signal. The Read-to-FIFO signal of Figure 4-3 represents the output of the nand gate.

The active-low Read signal produces a pulse which follows the Word Clock with a maximum of 15 + 55 + 15 = 85ns delay. A careful analysis of this signal after the 17th word is necessary. The flip-flop only requires a setup time of 20ns, and the PDP-629 Enable signal is sure to be low within 20ns of the falling edge of the 17th pulse of the Word Clock. The gated Enable signal will then go low a maximum of 40ns following the rising edge of the inverted Word Clock. A positive Read pulse will be generated by the monostable following the rising edge of the 17th word of the inverted Word Clock. The typical delay for the monostable is 35ns with no minimum value given. This means that it is possible for this positive Read pulse to overlap the gated Enable by approximately 5ns in the worst case. This overlap would not be sufficient in length to cause the FIFO to read out another word since its duration would be much less than the required 120ns. Figure 4-3 shows that there is no Read pulse sent to the FIFO following the 17th pulse of the Word Clock.

G. DATA LATCH REQUIREMENT

The PCM encoder requires that digital data be stable a minimum of 5μs following the falling edge of the Word Clock, for an undetermined amount of time until the next Word Clock transition. This period of time amounts to 45μs during which the data is latched by the PCM encoder at some point. The most reliable way to hold digital data for that length of time is with the use of a latch. Two octal latches were necessary to latch all ten bits of the data word, and their technical data is included in Appendix G. The latches are transparent while their control signal is high. Data which has been setup by 5ns is latched into the device if it is held for 20ns past the falling edge of the Latch signal.

The key to ensuring that valid data is latched, is to make the falling edge of the Latch signal occur when data is valid out of the FIFO. This is simply done with another monostable multivibrator, which allows control of the timing of the falling edge of the pulse. A Latch pulse duration of 2.1μs was selected to fulfill these requirements, and circuit components were selected according to Equation 4-1. This ensures that valid data from the FIFO will be setup and latched into the latches.

It is not necessary for the Latch pulse to occur only when the Enable signal is asserted, as was the case with the Read signal. Asserting extra Latch pulses will not result in a loss of data by the instrument. The Ground Support Equipment (GSE), which will be discussed in Chapter V, uses the Latch pulse for data acquisition as a handshaking signal. This requires that the Latch pulse to the integrated circuit occur only with the Read pulse to the FIFO so that a latch signal only occurs when a new data word is read. This is an artificial requirement imposed on the interface circuit due to the test setup in the laboratory. It does not impose any limitations on the interface circuit operation in the rocket, and provides for the simplest method of data acquisition in the lab.

The Latch signal is nanded with the gated Enable signal to produce a negative Latch signal which is only asserted when the enable signal is active. Since the integrated circuit requires a positive pulse, the signal is fed through both inputs of another nand gate. The nand gate output is used as the Latch signal to the integrated circuit. Two levels of nand gates impose a maximum delay of 30ns on the original generated Latch signal, but this delay is not a concern in the timing of the circuit.

H. BUFFERING OF CONTROL LINES

Several of the control signals generated in the interface circuit, Read, Write, Reset, etc., must travel on wires outside of the metal box which houses the interface circuit. This was due to the fact that the circuit had to be constructed on two printed circuit boards. Some control signals had to pass from one board to the other via external wiring. These signals were buffered prior to sending them out of the interface circuit enclosure in an effort to prevent any external noise imposed on these lines from getting back into the interface circuit. In addition, some control signals are sent out on the cable which connects the MUSTANG payload to the rocket telemetry section. This was considered necessary since the MUSTANG instrument is under vacuum the entire time that it is attached to the rocket. In order to determine if the instrument is functioning properly prior to launch, or to troubleshoot the interface circuit while under vacuum, these control signals must be fed out through the telemetry cable. It was considered prudent to buffer these signals due to the significant length of cable runs to which these signals would be exposed. A single octal buffer chip was all that was necessary to protect these signals. Technical data for the buffer is included in Appendix H.

This completes the requirements for the design of the revised electronic interface circuit. The circuit diagram for the final design is included as Figure 4-4.

I. INSTRUMENT GAIN CONTROL VOLTAGE

The instrument gain control voltage portion of the interface circuit is electrically separate from the previously described circuit. This part of the interface is called the high voltage circuit since it supplies the control voltage to the high voltage power supply. Chapter II described the necessity for the high voltage portion of the MUSTANG instrument to only be energized when the instrument is under full atmospheric or full vacuum conditions. Harmful arcing may occur if the high voltage power supply is energized under partial vacuum [Ref. 4:p. 43]. Technical data for the high voltage power supply is included in Appendix C.

The high voltage power supply is powered from +5V, and requires a control voltage between 0 - 10V to control the high voltage output to the MUSTANG image intensifier. The gain of the MUSTANG instrument is an exponential function of this control voltage. The +5V power supply is energized separately from the power to the rest of the interface circuit. The function of this portion of the interface circuit is to provide a regulated control voltage. Since two separate gain values were desired for this flight, two different control voltages

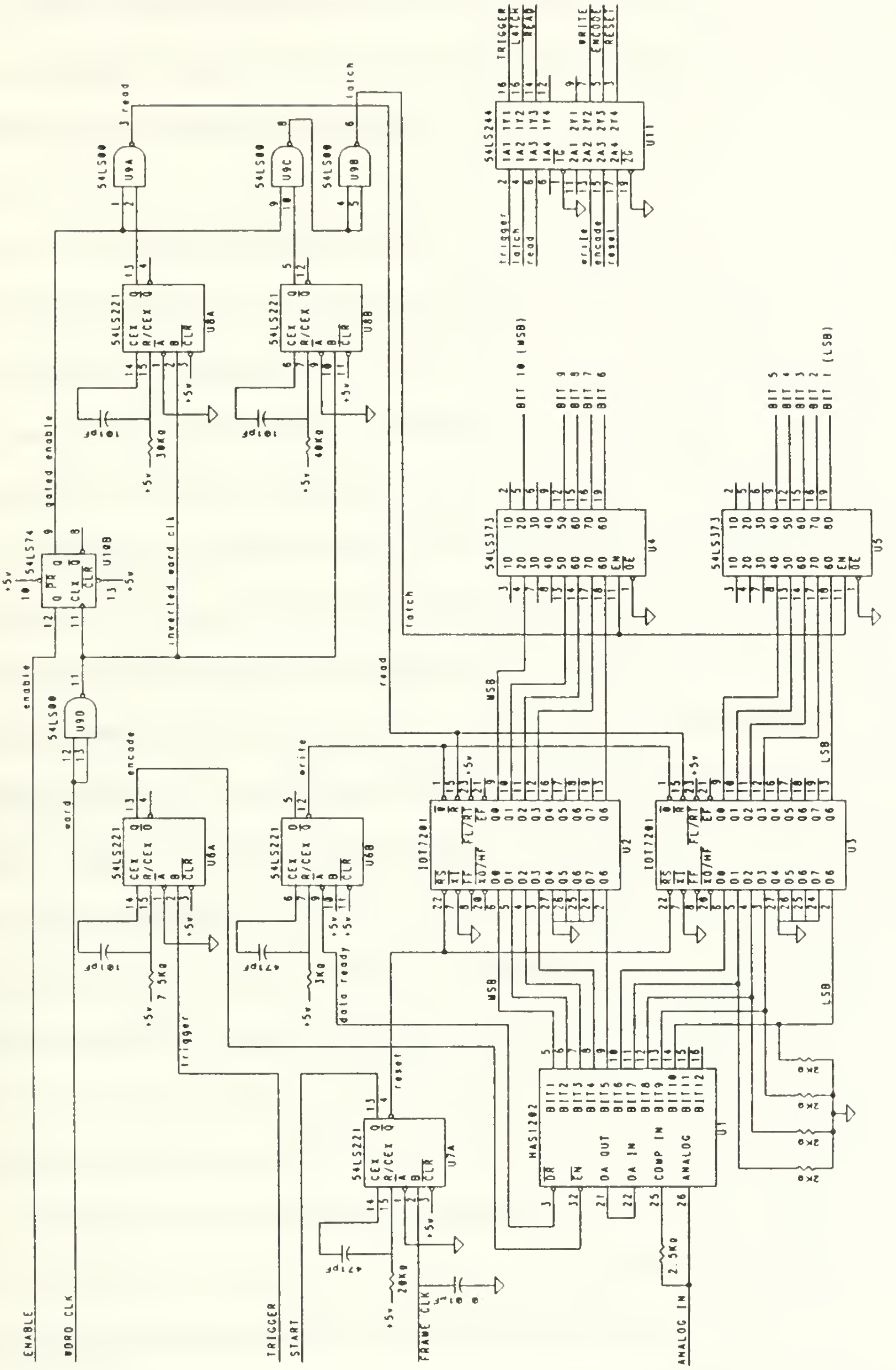


Figure 4-4 MUSTANG Electronic Interface Circuit Final Design

had to be created on the high voltage portion of the interface circuit. A method must also exist to select one of the two control voltages while the rocket is in flight. Two alternatives were investigated to supply the required control voltages.

1. Two Regulated Voltages and an Analog Switch

A single adjustable voltage regulator was used in the original interface circuit to supply the single control voltage. It would not be difficult to add a second voltage regulator that was adjusted to the second control voltage. The two analog control voltages could then be supplied to an analog switch. An additional telemetry signal would be required to select the output of the analog switch. This alternative involved adding many components to the circuit. Each voltage regulator required several resistors and capacitors to set the output voltage. Each output voltage would require a buffer in order to provide a constant voltage. An analog switch is available as a small integrated circuit package; however, it requires a +15V and -15V power supply. The current rocket configuration supplies only +5V and +15V to the high voltage portion of the interface circuit. This alternative would require a modification to the existing rocket configuration to supply -15V and a gain select signal to the high voltage portion of the circuit. It would require a large amount of board space for all of the additional components, and would be less reliable due to all of the added components. For these reasons, this alternative was not selected.

2. Digital-to-Analog Converter

A digital-to-analog (D/A) converter could perform the task of supplying two different analog voltages if a combination of the input bits were used as the gain select signal to change the output voltage. A sophisticated D/A converter could provide all of the functions of the two voltage regulators and an analog switch in a single integrated circuit package. For these reasons, the Analog Devices AD-667 D/A converter was selected to perform this function. Technical data for the AD-667 is included in Appendix E. This device performs 12-bit D/A conversion in an acceptable 3µs. The conversion time is not critical since the gain will only change once at the rocket flight apogee and again at 100km altitude on the down leg. The device provides its own stable, buried zener reference voltage, and a buffer on the output analog voltage. This ensures a stable voltage out of the device, regardless of the amount of current drawn by the load. The device also provides a latch on the input digital data so that it is not critical to keep the digital inputs stable at all times.

This single D/A converter supplied all of the necessary characteristics of a stable, selectable control voltage. The only drawbacks of this alternative were the relatively high cost of such a sophisticated device, and the requirement for a +15V and -15V power supply. Both alternatives required a modification to the existing rocket configuration to supply -15V and a gain select signal to the high voltage portion of the circuit. The D/A converter provided a smaller board area and a higher reliability, so it was chosen as the method for generating the control voltages.

The existing Frame Clock was used to latch the digital data into the D/A converter. Since data is latched into the device on a rising edge, the Frame Clock was inverted by supplying it to both inputs of a nand gate. The nand gate output was used as the latch signal to the D/A converter. This ensured that the gain would be constant for an entire frame of data. It also allowed the data to be latched every frame in case an erroneous value were latched due to noise. This would cause only one frame of data to be in error rather than the data for the entire flight.

It was determined from the data of the previous MUSTANG flight that the control voltages necessary for proper instrument gain were approximately 9.40V and 9.70V. The 10.00V reference voltage in the 12-bit D/A converter meant that the analog voltage resolution was 2.44mV. This was more than adequate to provide the two required control voltages. A D/A converter with less input bits could have provided this resolution; however, a device with all of the other capabilities of the AD-667 was not available. The proper control voltages could be obtained by changing only a single bit into the D/A converter as shown in Figure 4-5.

MSB Bit Number LSB

11	10	9	8	7	6	5	4	3	2	1	0		
1	1	1	1	1	0	0	0	1	0	0	0	⟶	9.7047v
1	1	1	1	0	0	0	0	1	0	0	0	⟶	9.3923v

Gain Select Signal

Figure 4-5 Control Voltage to High Voltage Power Supply

The Gain Select signal from the rocket telemetry section would be applied to Bit 7 of the D/A converter. A logic zero on this line would select low gain and a logic one (+5V) would select high gain. All other digital bits into the D/A converter would be hardwired to ground or the +5V high voltage power supply.

The relay which energizes the high voltage power supply to the MUSTANG payload causes +5V, +15V and -15V to be supplied to the high voltage portion of the interface circuit. This causes the control voltage to be produced and applied along with +5V to the high voltage power supply on the MUSTANG instrument. The circuit diagram for the high voltage portion of the final interface circuit is shown in Figure 4-6.

J. CIRCUIT POWER REQUIREMENTS

The power requirements of the MUSTANG electronic interface circuit as well as the MUSTANG instrument itself must be known prior to time of flight. This allows for proper selection of the flight batteries for the rocket mission. A worst case evaluation can be made based on figures supplied in each components technical data. Some databooks supply the typical and maximum power consumption. Others give only power supply current drawn, in which case the power consumption can be calculated by multiplying by the supply voltage. Table 4-1 is a compiled list of the typical and maximum power dissipated in each of MUSTANG's components.

The power consumption figures in Table 4-1 are totals for the number of components used in the interface circuit (i.e., there are three 54LS221 integrated circuits in the electronic interface, so the table reflects the power consumed by all three together).

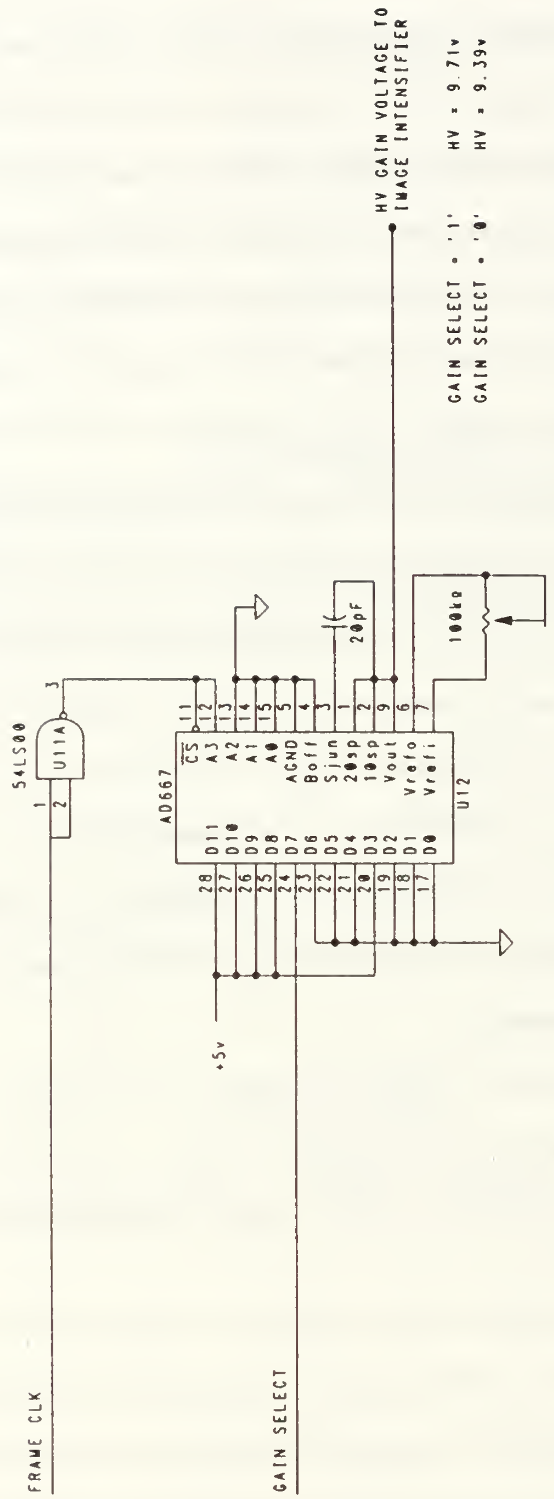


Figure 4-6 MUSTANG High Voltage Control Circuit Final Design

TABLE 4-1 MUSTANG POWER REQUIREMENTS

Component	Typical Power	Maximum Power
54LS00	0.024 watt	0.044 watt
54LS74A	0.020	0.040
54LS221	0.285	0.405
54LS244	0.135	0.230
54LS373	0.270	0.400
IDT-7201	0.700	1.000
HAS-1202	1.900	2.750
AD-667	0.420	1.000
Driver/Amplifier	1.200	1.500
HV Power Supply	0.445	0.445
Total Power Reqd.	**5.399 watt**	**7.814 watt**

V. GSE DESIGN AND MODIFICATION

The MUSTANG ground support equipment (GSE) provides two functions. It allows for testing and calibration of the MUSTANG instrument in the laboratory, and it allows for checkout of the MUSTANG instrument during installation on the sounding rocket, prior to flight. In the laboratory, the GSE must simulate all functions provided by the rocket during flight. During installation on the rocket, the GSE must not interfere with payload integration, but at the same time collect enough data to ensure the MUSTANG is operating properly.

The MUSTANG GSE consists of a Macintosh II computer with additional National Instruments data acquisition boards, an interface box and a power supply. The interface box was built by Naval Postgraduate School technicians, and the software was written by Professor Dave Cleary prior to the first MUSTANG launch. No real documentation exists for these original programs or the interface box construction. The operation of the interface box electronics was deduced during the course of this thesis work. The electronics were modified both to correct for shortfalls in performance, as well as to adapt to changes in the upcoming MUSTANG flight. The software programs were rewritten in an attempt to make them both more efficient and more user friendly.

This chapter is meant to serve as a guide to how the MUSTANG GSE really works in its current configuration. Hardware and software operation will be discussed in their entirety. Mention will be made where modifications were made as a result of this thesis work.

A. FUNCTIONS OF LABORATORY GROUND SUPPORT EQUIPMENT

The laboratory GSE must provide two functions. It must provide the same clock synchronization signals that the MUSTANG receives from the PCM encoder during flight. This provides a flight environment for testing the MUSTANG instrument. It must also collect data from the MUSTANG instrument just as the PCM encoder would in flight. A method to display this data is also necessary, in order to determine if the MUSTANG is operating properly. These two functions are provided by the Macintosh II computer and National Instruments (NI) data acquisition boards. The interface box is necessary for synchronizing all of the clock signals, and for providing a medium to transfer signals from the NI data acquisition boards to the MUSTANG flight instrument .

1. PCM Encoder Clock Synchronization Signals

The Macintosh II computer provides the clock synchronization signals via two NI data acquisition boards. The NI boards are all Macintosh NuBus cards and are attached to each other by a Real-Time System Integration (RTSI) bus connector. This allows for signal passing between the cards without having to wait for the Macintosh bus. An NB-DMA-8-G board has a counter/timer which provides the master system clock over the RTSI bus to the other boards. An NB-MIO-16 board provides all of the PCM encoder clocks synchronized to the system clock via its counter/timers. Signals provided by the MIO board are as follows.

- 200kHz, 5μs period, Bit Clock
- 20kHz, 50μs period, Word Clock

- 1.25kHz, 800μs period, Enable Clock
- 19.53Hz, 51.2ms period, Frame Clock

The 50-pin input/output (I/O) connector to the MIO board provides the clocks at the pins indicated in Figure 5-1. The Word Clock is high for one Bit Clock period, and low for the next nine periods. This accommodated the ten-bit words as described in Chapter II. The Bit Clock and Word Clocks produced by the GSE are shown in Figure 5-2. The signals in this figure are actually in error, since the rising edge of the Word Clock should correspond to the rising edge of the Bit Clock. The GSE modified to correct this problem as described in a later section of this chapter. This figure also shows that the amount of noise in these clocks is excessive. The majority of this noise does not originate from the NI boards, but is added in the GSE interface electronics. The amount of noise present in the clock signals on the sounding rocket is unknown. It was decided that the MUSTANG electronic interface circuit should be designed to be robust enough to operate in this level of noise, rather than reducing the noise in the GSE interface electronics. In this sense, the MUSTANG interface circuit design considered a worst case noise environment.

Figure 5-3 shows the Enable signal produced by the GSE in relation to the Word Clock. The Enable signal is high for 16 cycles of the Word Clock and then low for the next 16 cycles. As in the sounding rocket, data is only read from the MUSTANG instrument when the Enable signal is high. Unlike the sounding rocket, the Enable signal is perfectly synchronous with the Word Clock since it is produced by the NI boards. The problems experienced with the PD-629 Enable signal described in Chapter III are not present in the GSE configuration. Figures 5-4 and 5-5 show that the rising and falling edges of the

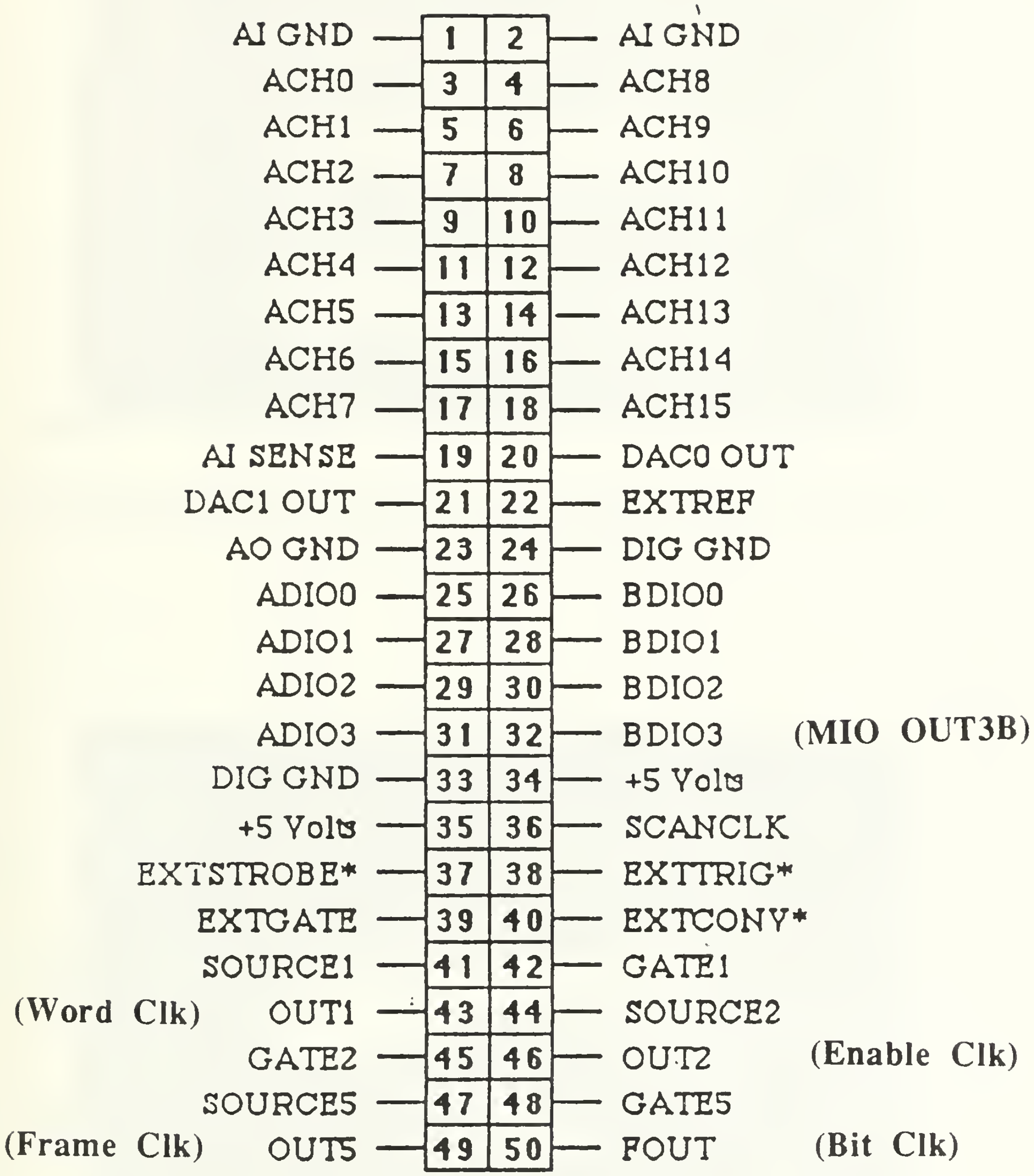


Figure 5-1 NB-MIO-16 I/O Connector [After Ref. 7:p. 2-13]

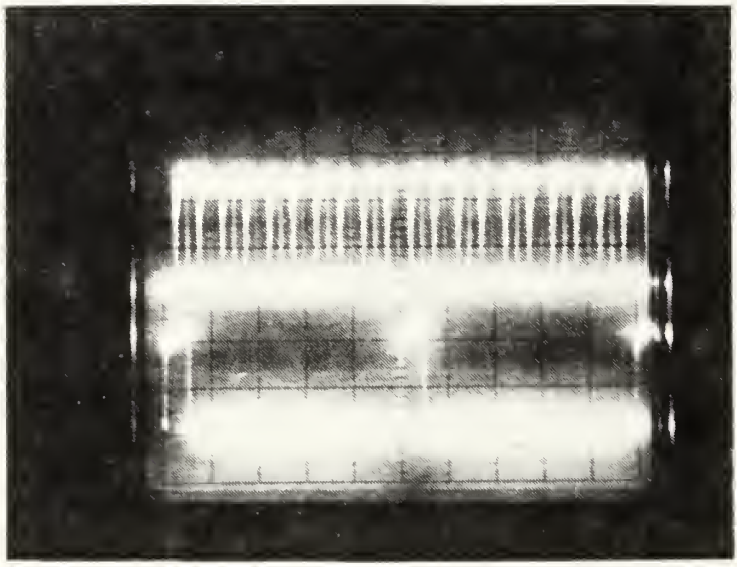


Figure 5-2 Bit Clock (top) and Word Clock (bottom)

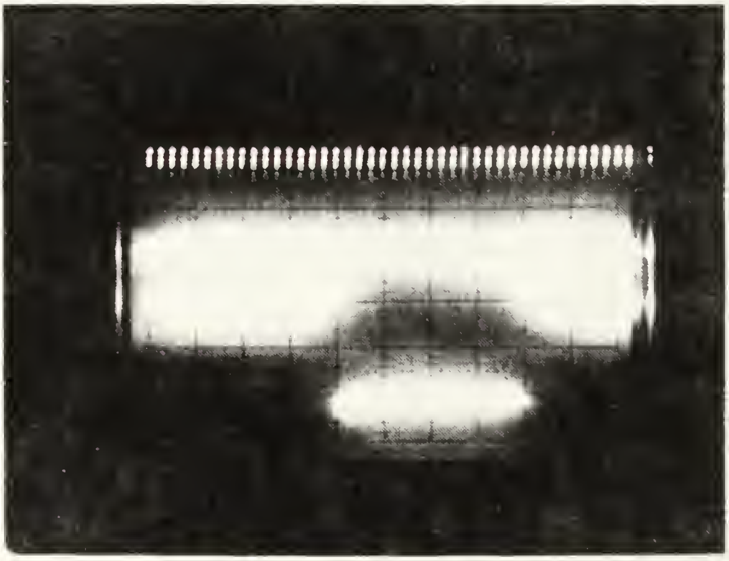


Figure 5-3 Word Clock (top) and Enable command (bottom)

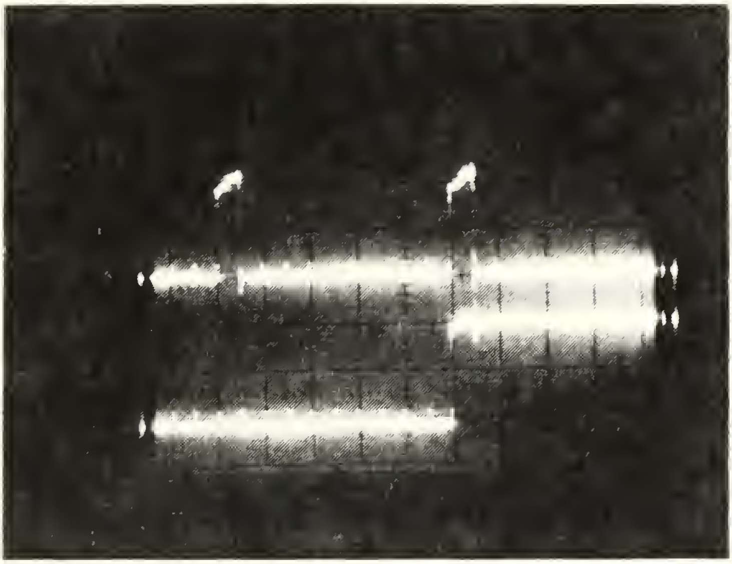


Figure 5-4 Magnified Word Clock (top) and Beginning of Enable command (bottom)

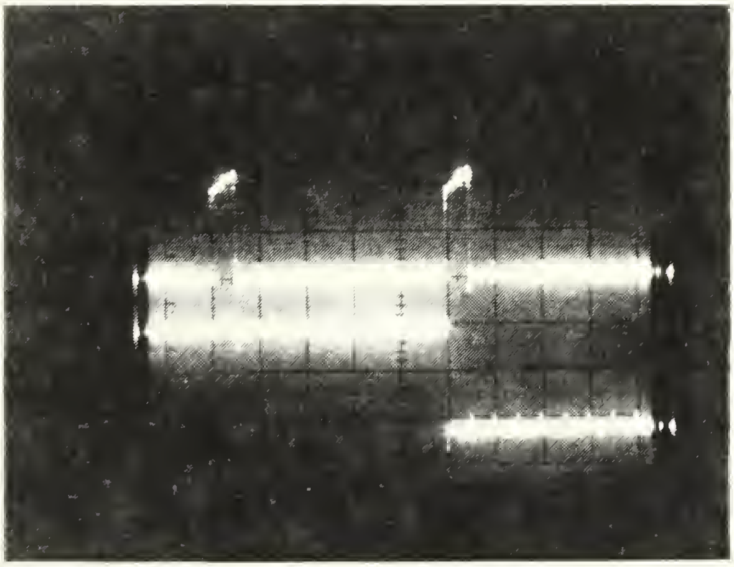


Figure 5-5 Magnified Word Clock (top) and End of Enable command (bottom)

Enable signal are synchronous with the rising edge of the Word Clock. An effort was made to produce an Enable signal in the GSE that looked like the PD-629 Enable, and is discussed in a later section. The Frame Clock produced by the GSE is shown later in Figure 7-5, and is high for one Word Clock period in 1024 .

2. Collection and Display of a MUSTANG Spectrum

The GSE also collects the data read out from the MUSTANG interface circuit. Digital data is latched into an NI NB-DIO-32F data acquisition board in the Macintosh II computer. The collected data is displayed on the Macintosh screen as a MUSTANG spectrum. The 512 photodiodes in the linear image sensor are represented by the 512 pixels displayed in the MUSTANG spectrum shown in Figure 5-6. LabVIEW 2.0 software published by National Instruments is used to create this screen display. The LabVIEW software is compatible with all of the NI data acquisition boards. The following sections describe how the programs are written to provide the telemetry clocks and acquire the data for display of a MUSTANG spectrum on the GSE computer.

B. LABVIEW 2.0 PROGRAM FOR DATA ACQUISITION

The basic entity of a program in LabVIEW is know as a virtual instrument or VI. This is an object oriented programming language in the sense that programs or VIs are represented on the Macintosh screen as small icons. A VI is made up of two parts. The front panel is the program interface with the user. The block diagram represents the mechanics or code of the program. A VI is constructed by filling its block diagram with other sub-VIs or basic elements, and then wiring them together with a wiring tool. Calls to multiple sub-VIs may be nested several levels deep. Regular program structures such as Case structures, Sequence structures, For loops and While loops are all implemented in LabVIEW in an object oriented fashion. A basic knowledge of the LabVIEW program is assumed in the following discussion.

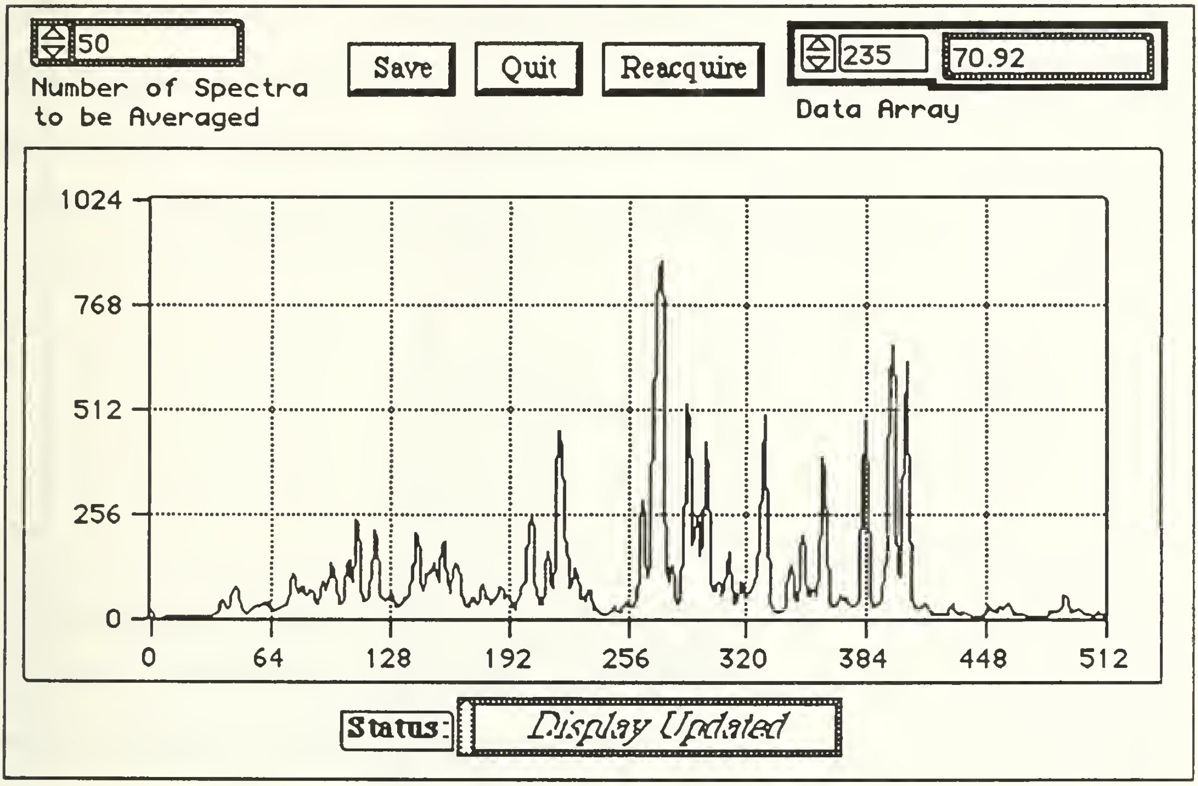


Figure 5-6 Data Acquisition Computer Screen (Platinum Lamp Spectrum)

1. Hardware Configuration

Many LabVIEW VIs which interface with the NI data acquisition boards are already included in a LabDriver VI library which is provided by National Instruments. All of the LabDriver library VIs discussed in this chapter are listed in Table 5-2 at the end of the chapter. This table provides a cross-reference page number where the VI can be found in Reference 8. As mentioned previously, an NB-DMA-8-G board is utilized to create the master system clock. No explicit use is made of the direct memory access (DMA) features of the board in this application. The NB-MIO-16 board is only used to create the four clock signals provided by the PCM encoder. It has the capability to provide analog-to-digital signal processing, but this is not utilized in the GSE. The NB-DIO-32F board simply provides a digital input port to read in the data from the MUSTANG interface circuit. Data is latched into the board as controlled by handshaking signals. The current NuBus address locations for the data acquisition boards are as follows.

• NB-DMA-8-G	NuBus slot #2
• NB-MIO-16	NuBus slot #3
• NB-DIO-32F	NuBus slot #4

2. Lab Software

The original GSE LabVIEW programs were written as separate entities which had to be run separately, and in the correct sequence in order to test the MUSTANG. The GSE programs have been revised so that all necessary VIs are accessed from within a single main VI. This main VI has been organized to be more user friendly. To take calibration data with the MUSTANG, the user need only click a few labeled buttons on the screen to see the displayed spectrum. This allows students to collect and study the MUSTANG calibration data without having knowledge of the electronic interface circuit or of the LabVIEW software.

A hierarchy of all sub-VI calls in the Main GSE program is included as Figure 5-7. Each VI is represented by its appropriate icon in the figure. The main VI calls three sub-VIs. Each of these VIs in turn call other sub-VIs as depicted in the figure. The following sections will describe the operation of the

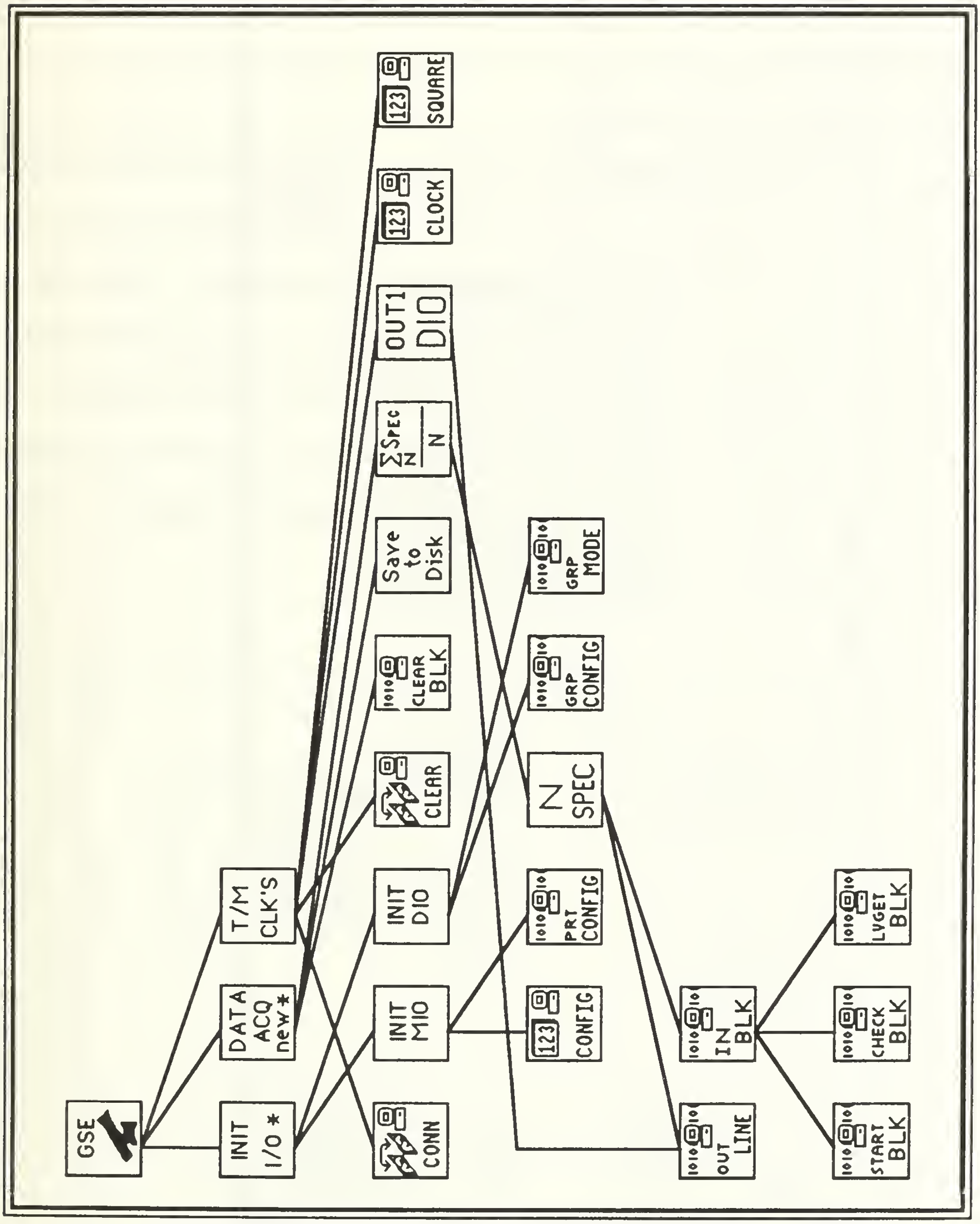


Figure 5-7 VI Hierarchy in the Main GSE Program

VIs represented by each of the icons in the hierarchy. Operation of the LabVIEW library VIs, where obvious from the LabVIEW user manuals, will not be explained.

a. Main GSE Program

The Main GSE VI includes all previous GSE programs, which are now referred to as sub-VIs. The front panel of the Main GSE VI is shown in Figure 5-8. Several labeled buttons are shown on the left side. When the user clicks the mouse on the button, the sub-VI is executed to accomplish the task. A status window is shown which updates when a called sub-VI has completed. This tells the user what action has been accomplished by virtue of his clicking a button. The operation of the main VI is shown in its block diagram, which is included in Figure 5-9 and Figure 5-10.

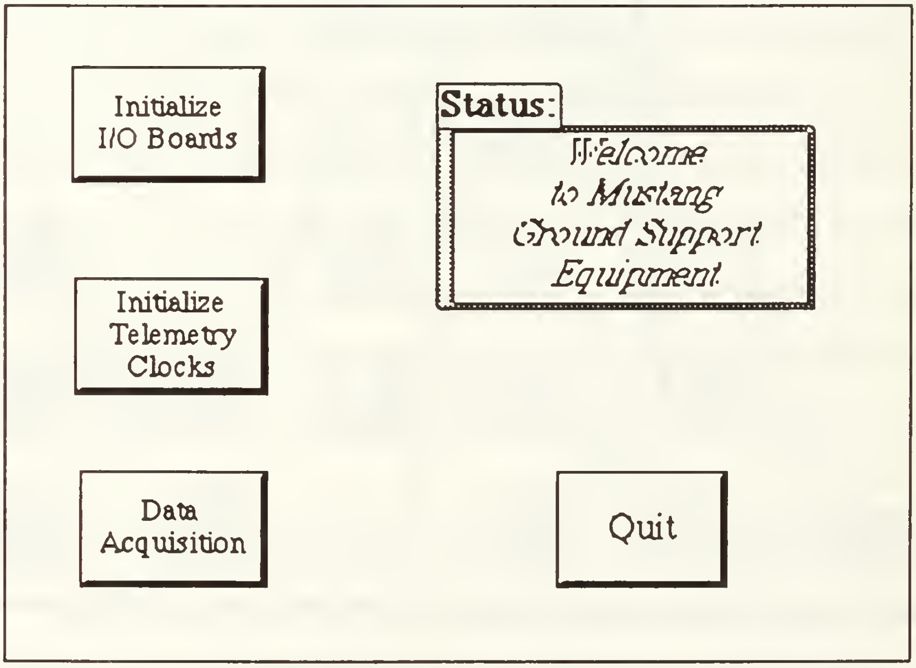

Initialize I/O Boards
Initialize Telemetry Clocks
Data Acquisition
Status:
Welcome to Mustang Ground Support Equipment
Quit

Figure 5-8 Main GSE VI Front Panel

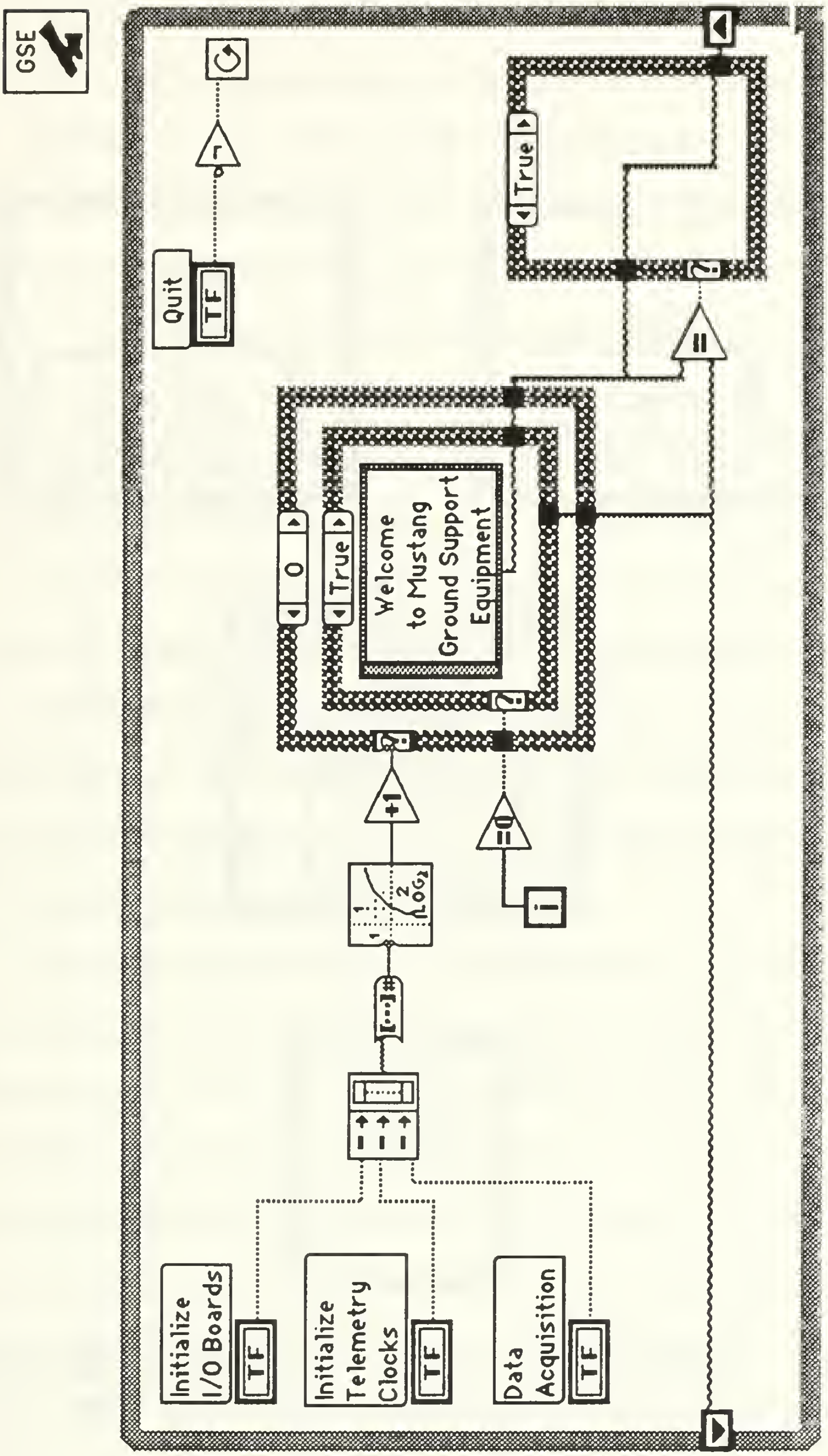

GSE
Quit
TF
True
0
True
Welcome to Mustang Ground Support Equipment
LOG2
+1
i
Initialize I/O Boards
TF
Initialize Telemetry Clocks
TF
Data Acquisition
TF

Figure 5-9 Main GSE VI Block Diagram

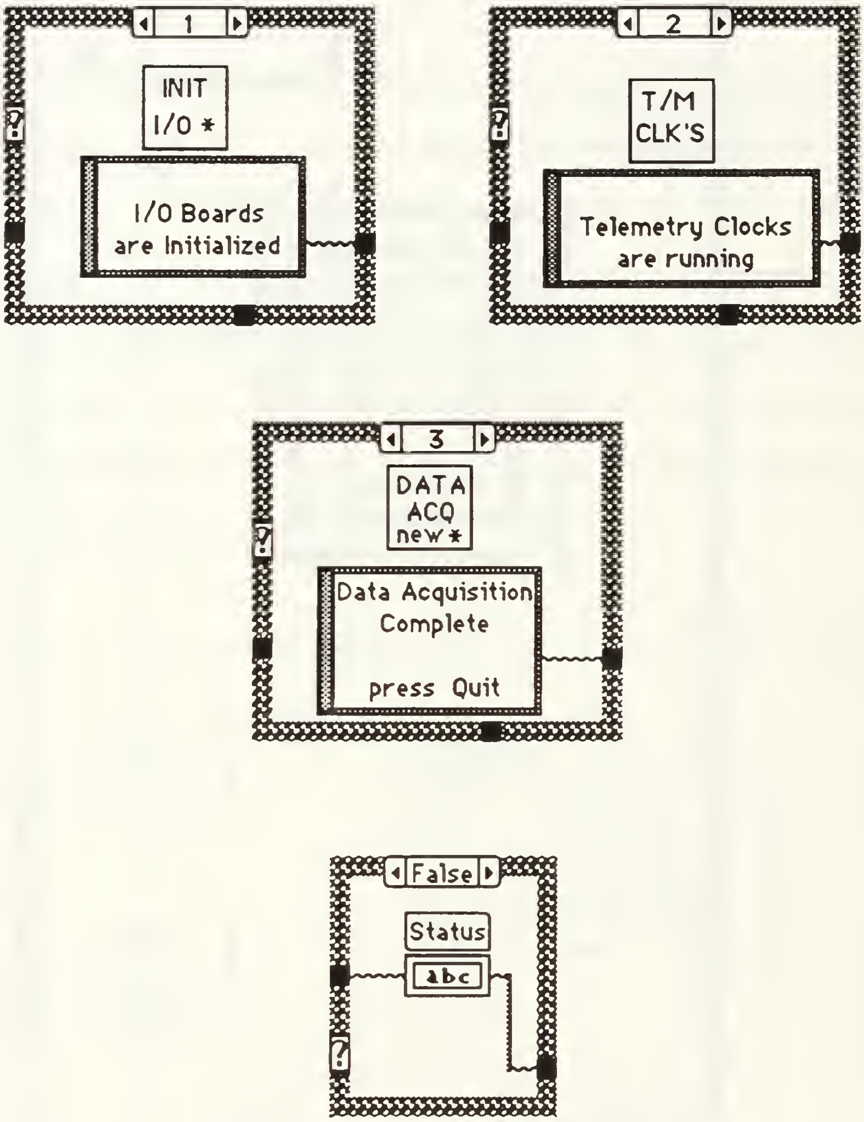


Figure 5-10 Main GSE VI Block Diagram Subsequent Cases

All buttons on the front panel are of the spring latch type. This means that when a button is depressed by clicking the mouse, the control changes to the new value and remains there until the program reads the new value once, or the mouse button is released, whichever occurs *last*. This means that even a quick click of the mouse button will cause the button to be read at least one time in the depressed position without the user having to hold down the mouse button.

The block diagram in Figure 5-9 shows the icon for the Main GSE VI in the upper right corner. This icon is not part of the block diagram. It was placed in the figure to allow for identification of the VI with which the block diagram is associated. This convention will be followed throughout this chapter. Some of the block diagrams in this chapter have been graphically edited to allow them to fit within the proper dimensions of this thesis format. All block diagrams illustrated in this chapter are functionally equivalent the the VIs running on the GSE computer. The names of LabVIEW functions and VIs will be shown in italics in this chapter.

The entire block diagram is enclosed in a while loop structure. Figure 5-10 simply shows the other cases not shown in Figure 5-9 for the three case structures present in the block diagram. When the Main GSE program is initiated, the while loop begins to run continuously. When the Quit button is depressed, a boolean TRUE value is passed to the inverter which sends a boolean FALSE value to the conditional terminal of the loop. This stops the while loop from running, and the Main GSE program stops execution. The iteration terminal of the while loop is wired to an *Equal to Zero* comparator function. The value of the iteration terminal is zero for the first execution of the loop, and is incremented by one on each loop iteration.

Indicators for the three buttons on the left side of the front panel are located on the left side of the block diagram. They send out a boolean FALSE value until the button is depressed, when a boolean TRUE value is sent out. The boolean variables from these three buttons are collected by the *Build Array Function*. This function creates an array of three boolean values. Array element zero is the value of the Initialize I/O Boards button. The output of this function is wired to the input of a *Boolean Array to Number* data type converter. This converts the binary number represented by the boolean array into a decimal number. The decimal number is passed to a *Logarithm Base Two* function and an *Increment* function. The output of the *Increment* function is wired to the selector of the case structure. This allows for depressing a single button to select a particular case in the block diagram as shown in Table 5-1. This technique is also demonstrated on page 6-3 of Reference 9.

TABLE 5-1 MAIN GSE VI CASE VALUES

Button Pressed	Array	Number	Base 2 Log	Case
None	000	0	-infinity	0
Init I/O Boards	001	1	0	1
Init T/M Clocks	010	2	1	2
Data Acq	100	4	2	3

When a particular case is selected, the contents of the case window in Figures 5-9 and 5-10 are executed. For cases one through three, this means execution of the sub-VI within the case structure. When the sub-VI completes, the text string is passed out of the case structure. Case zero is a special case executed when no buttons are depressed. This case window has another case structure inside it which is dependent on the number of while loop iterations. The first time the while loop executes, the iteration terminal value is zero. This produces a boolean TRUE out of the *Equal to Zero* comparator which selects the true case and the welcome message is sent out. Every other time the while loop executes, the iteration terminal value is something greater than zero, and the boolean FALSE case is selected. This case is not shown in Figure 5-10, but merely connects the input string at the bottom tunnel to the output string at the tunnel on the right side.

The shift register on the while loop structure holds the value of the text string to be displayed in the Main GSE status window, and passes it to the next iteration of the while loop. If this value were sent to the status window inside the while loop, it would be updated on the screen with every iteration. This causes the message to flash on the screen and does not present a good appearance. The additional case structure on the right side of Figure 5-9 prevents this message flicker by updating the status message only when it changes. The status window indicator is located in the FALSE case so it is only accessed when the *Equality* comparator indicates that the two inputs are not equal. This allows the status window display to only be updated whin its message changes.

When the Main GSE program is run for the first time, the iteration terminal value is zero and the welcome message is selected to come out of the first case structure. This is not equal to the null string which is the default initial value of the shift register. The status window is updated with the welcome message, and the welcome message is entered into the shift register. On the subsequent iterations of the while loop the iteration terminal is no longer zero so the false case is selected and the welcome message string is passed to both sides of the *Equality* comparator. This results in the string being passed straight through the true case structure, and the status window not being updated.

When a button is pushed, the appropriate case is selected and the sub-VI called and executed. When control returns to the Main GSE program, the new text string is sent out of the case structure causing the Equality comparator to result in a boolean FALSE. This updates the status window with the new message as before. On the following while loop iteration, the shift register has the new text string value so the status window will not be updated. This while loop continues to run in the background until the user depresses the Quit button.

b. Initialize I/O Boards

The first action to be taken, once the Main GSE program is running, is to click the Initialize I/O Boards button. This sub-VI must be run first to properly initialize the NI data acquisition boards in the Macintosh computer. The initialization only takes a second and the status window is updated to show that the I/O boards have been initialized. The block diagram for this VI is very simple, and it has not been included as a figure in this chapter. It merely contains two sub-VI icons. The two sub-VIs are Initialize MIO and Initialize

DIO which configure the counters and ports on the two data acquisition boards. Since the two sub-VIs are not within any program structure, they are executed concurrently.

(1) Initialize MIO. This sub-VI configures the three counters on the NB-MIO-16 data acquisition board. The counters are numbered one, two and five. Its block diagram is shown in Figure 5-11 and Figure 5-12. This block diagram utilizes a sequence structure in which a portion of the program is contained within a sequence frame. All operations within frame zero are first completed, and then control is passed to frame one. Four frames are contained within the block diagram. This is the method by which LabVIEW allows the programmer to ensure that certain events occur in a particular order.

The *CTR_Config* NI LabDriver VI is used in this block diagram to configure the MIO board counters. Frame zero configures counter number one, which will be the Word Clock. The counter is gated by a logic high level to allow for synchronization of the clocks. The edge mode was set to TRUE in order to correct the problem shown in Figure 5-2. The polarity was set to the default value of FALSE. These settings ensured that the rising edge of the Word Clock pulse would occur with the rising edge of the Bit Clock. The LabVIEW documentation is not very clear on how each of these settings will affect the counter output. A trial-and-error method was used to ensure that the clock signals were created properly. The following is a list of the counter number one characteristics.

- MIO board in NuBus slot #3
- MIO counter #1
- Input signal falling edges are counted
- Logic high level gates the counter

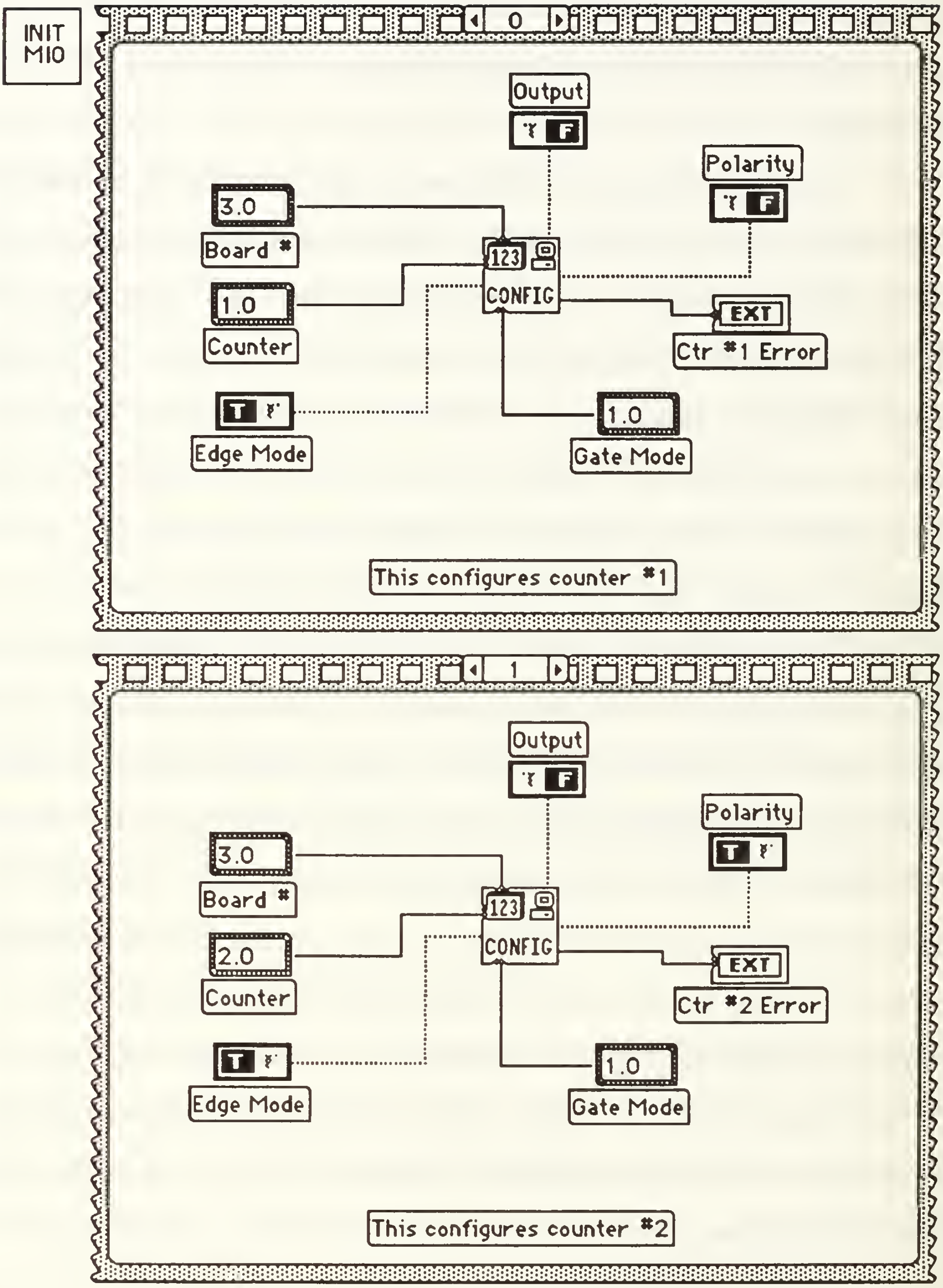
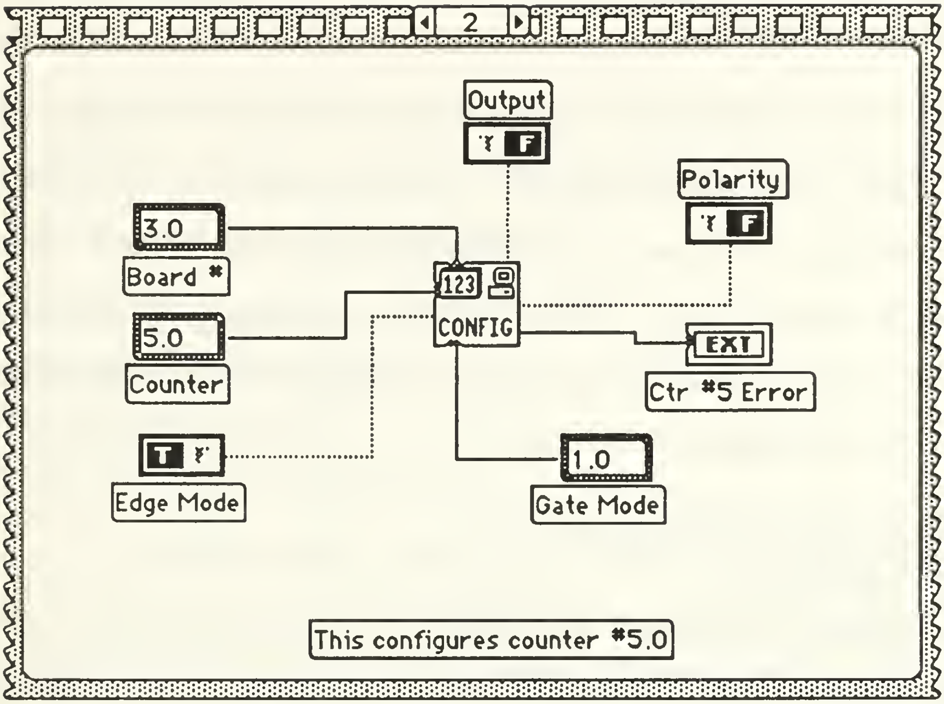


Figure 5-11 Initialize MIO VI Block Diagram



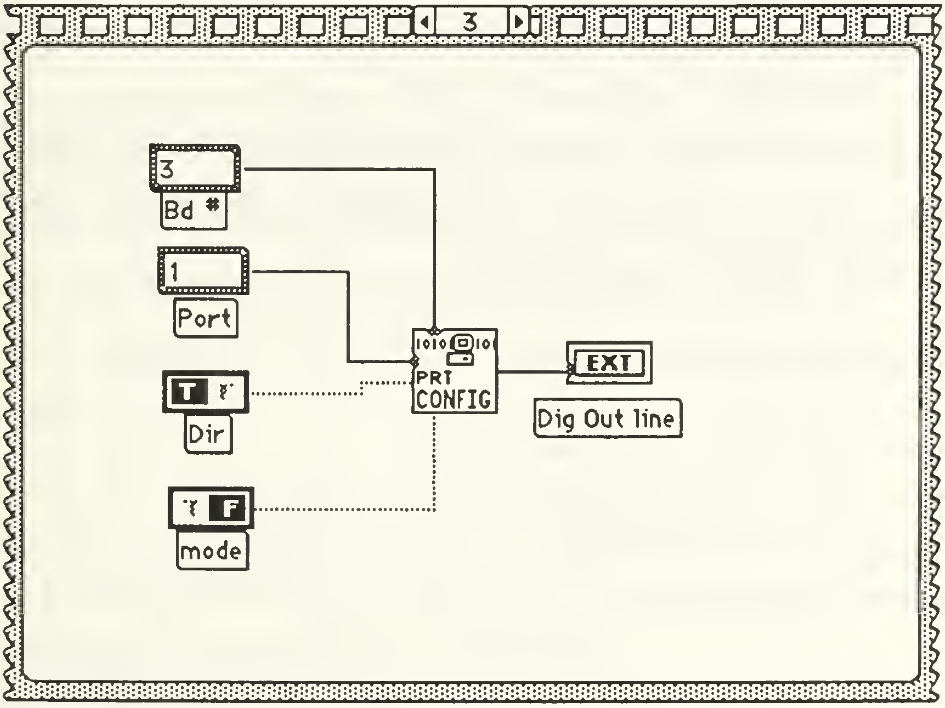


Figure 5-12 Initialize MIO VI Block Diagram (continued)

- TC toggle output type is used
- Positive logic output

Counter two is configured similarly in frame one as the Enable signal. The only difference is that its polarity is switched to be an inverted output. This ensures that the Enable signal will be low for the first 16 words of the frame of data. This is consistent with the actual telemetry clocks where the first 14 data words of the PCM matrix are for housekeeping signals. Counter two is configured as follows.

- MIO board in NuBus slot #3
- MIO counter #2
- Input signal falling edges are counted
- Logic high level gates the counter
- TC toggle output type is used
- Negative logic (inverted) output

Counter five is configured similarly as the Frame Clock in frame two. It has a positive logic output similar to the Word Clock in frame zero. It has the following characteristics.

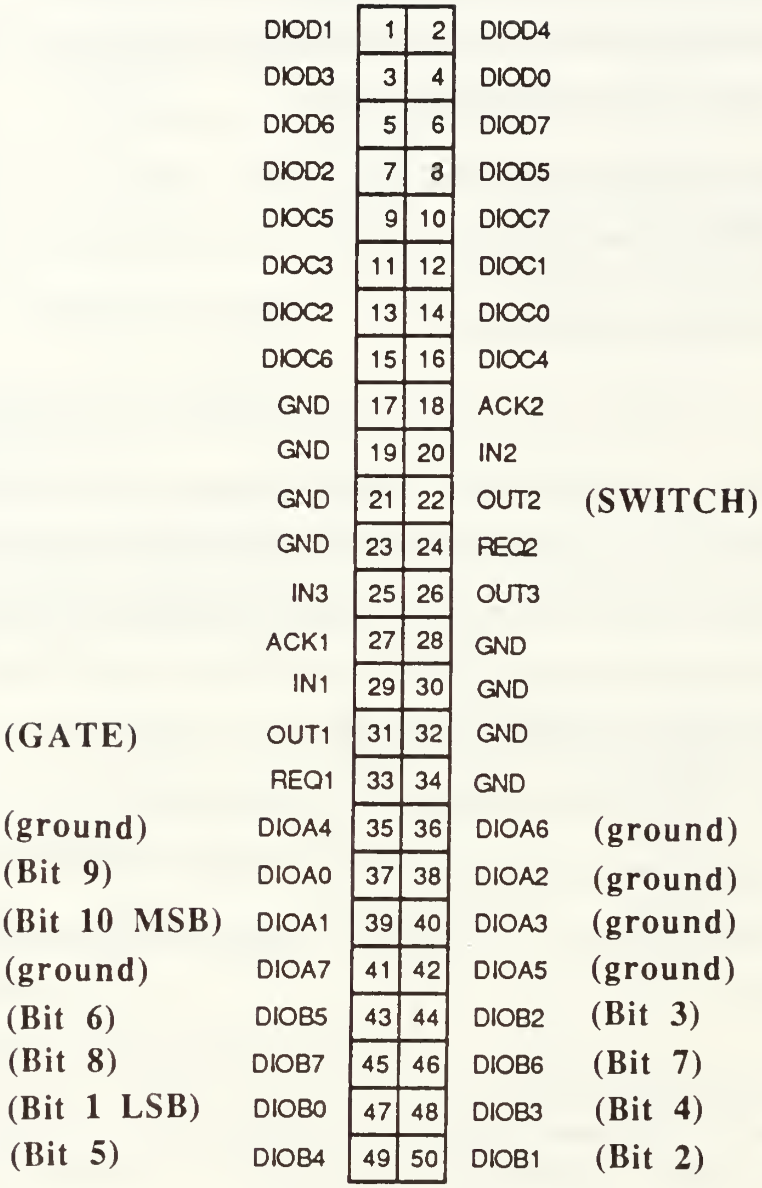
- MIO board in NuBus slot #3
- MIO counter #5
- Input signal falling edges are counted
- Logic high level gates the counter
- TC toggle output type is used
- Positive logic output

The last frame in the sequence calls the *DIG_Prt_Config* LabDriver VI. This configures the four-bit digital port BDIO on the MIO board as an output port. The BDIO port pins are shown in Figure 5-1. This step is only necessary when using the GSE at the launch site when the MUSTANG instrument is tested with the Launch GSE interface box. The inclusion of this frame does not affect performance when using the GSE in the laboratory so the frame is included all the time. Use of this digital output port is explained in a later section. The port is configured as follows.

- MIO board in NuBus slot #3
- Port #1 (BDIO) is configured
- Port configured as output
- No-handshaking (nonlatched) mode

(2) Initialize DIO. This sub-VI configures the digital ports on the NB-DIO-32F data acquisition board. The output connector for the DIO board is shown in Figure 5-13. The block diagram for this sub-VI is shown in figure 5-14. This VI also makes use of the sequence structure, and the program is contained in two sequence frames. The DIO board has 32 digital lines which can be configured as eight-bit ports for input or output. MUSTANG data words are ten bits long, so two ports are configured as a group for input of digital data. Six of the digital lines in the port are not used. Frame zero calls the *DIG_Grp_Config* LabDriver VI. This frame assigns two of the digital ports to a group as follows.

- DIO board in NuBus slot #4
- Group zero is the group of ports to be configured
- Port zero assigns 8-bit Ports zero and one to the 16-bit group zero
- Group size of two configures a 16-bit group
- Group configured as an input port



	DIOD1	1	2	DIOD4	
	DIOD3	3	4	DIOD0	
	DIOD6	5	6	DIOD7	
	DIOD2	7	8	DIOD5	
	DIOC5	9	10	DIOC7	
	DIOC3	11	12	DIOC1	
	DIOC2	13	14	DIOC0	
	DIOC6	15	16	DIOC4	
	GND	17	18	ACK2	
	GND	19	20	IN2	
	GND	21	22	OUT2	(SWITCH)
	GND	23	24	REQ2	
	IN3	25	26	OUT3	
	ACK1	27	28	GND	
	IN1	29	30	GND	
(GATE)	OUT1	31	32	GND	
	REQ1	33	34	GND	
(ground)	DIOA4	35	36	DIOA6	(ground)
(Bit 9)	DIOA0	37	38	DIOA2	(ground)
(Bit 10 MSB)	DIOA1	39	40	DIOA3	(ground)
(ground)	DIOA7	41	42	DIOA5	(ground)
(Bit 6)	DIOB5	43	44	DIOB2	(Bit 3)
(Bit 8)	DIOB7	45	46	DIOB6	(Bit 7)
(Bit 1 LSB)	DIOB0	47	48	DIOB3	(Bit 4)
(Bit 5)	DIOB4	49	50	DIOB1	(Bit 2)

Figure 5-13 NB-DIO-32F I/O connector [After Ref. 10:p. 2-2]

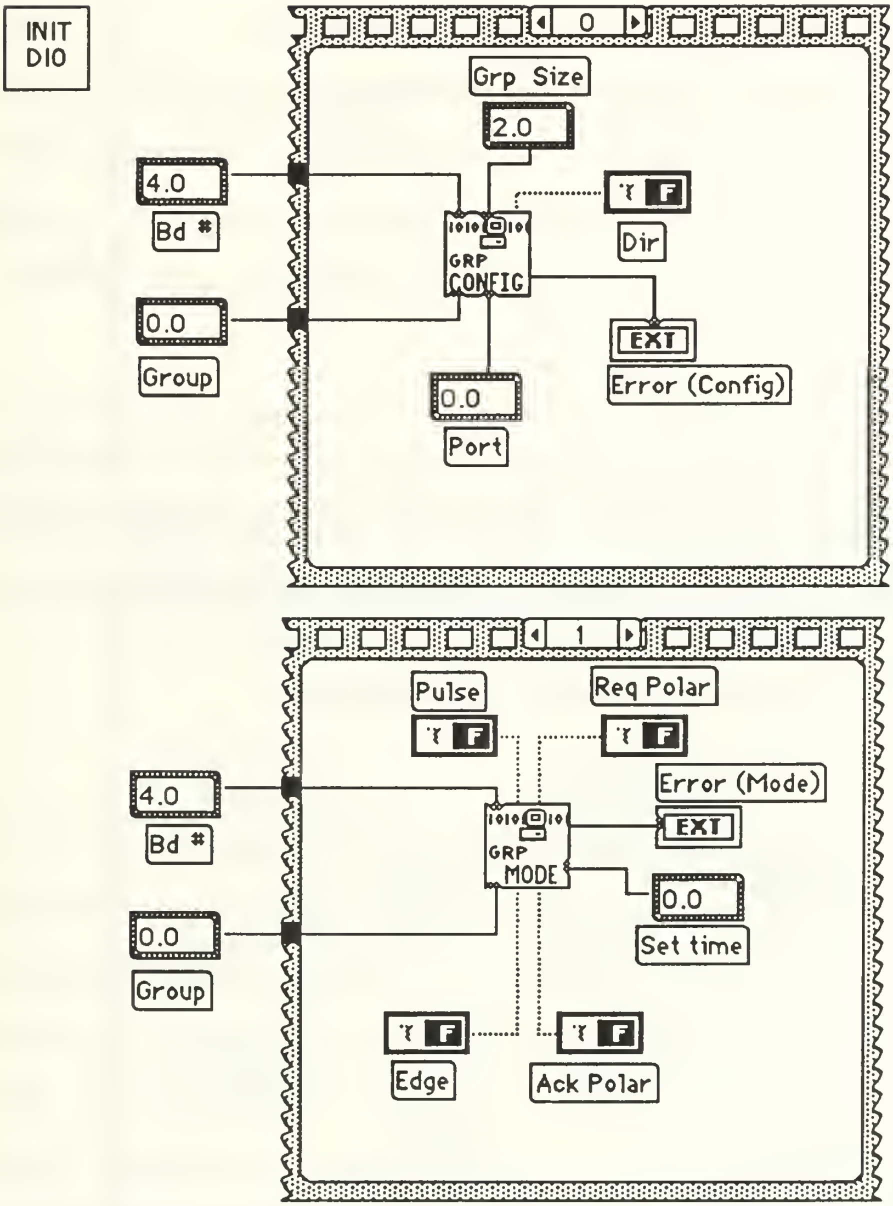


Figure 5-14 Initialize DIO VI Block Diagram

The handshaking method by which digital data will be latched into the input port is established in frame one. Pin number 33, labeled REQ1, on the NB-DIO-32F connector of Figure 5-13 is the handshaking signal sensed by this group. The origin of this signal is discussed in a later section of this chapter. The group sends out a handshaking acknowledgement signal, called ACK1, on pin number 27 which is not used by the electronic interface circuit. The *DIG_Grp_Mode* LabDriver VI is called for the purpose of establishing the handshaking method, and configures the handshaking mode as follows.

- DIO board in NuBus slot #4
- Group zero established in frame zero is the group to be configured
- Group is configured to recognize rising edge pulsed handshake signals
- Group is configured for active-high polarity handshake acknowledge signals
- Group is configured for active-high polarity handshake request signals
- Group is configured for level handshake signals
- No data settling time is allowed for the group

c. Telemetry Clocks

Once the data acquisition boards have been initialized, the next step is to run the clocks so that they provide the correct telemetry signals to the MUSTANG instrument. This is done by clicking the Initialize Telemetry Clocks button on the Main GSE front panel. The block diagram for this VI is a series of ten frames which are illustrated in Figures 5-15 through 5-19. The first two frames configure the RTSI bus to send the master clock signal from the DMA board to the MIO board. Frame zero clears all signal assignments to the RTSI bus by calling the *RTSI_Clear* LabDriver VI. Frame two calls the *RTSI_Conn* LabDriver VI to assign signals to the RTSI bus as follows.

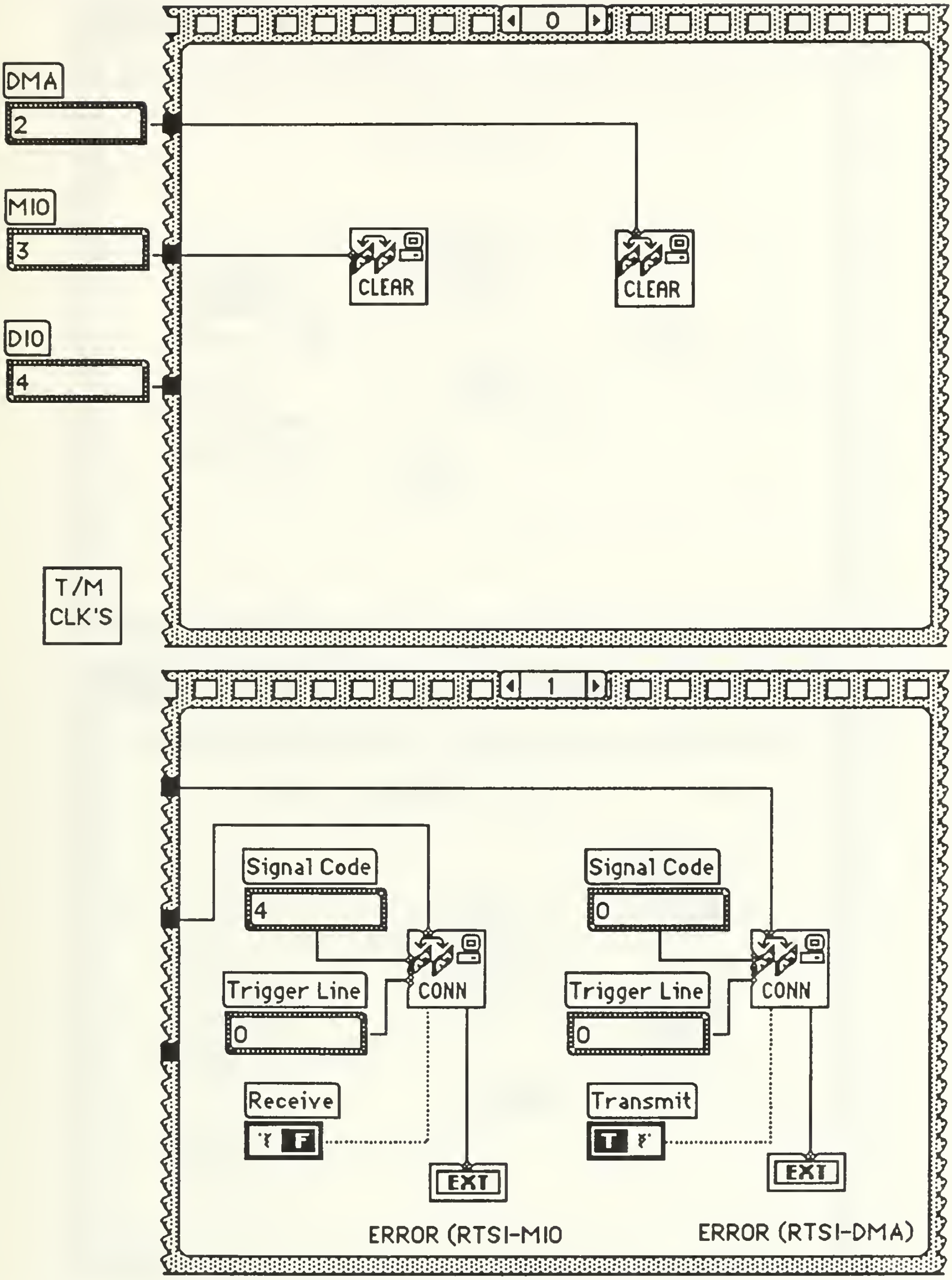


Figure 5-15 Telemetry Clocks VI Block Diagram (Frames 0 and 1)

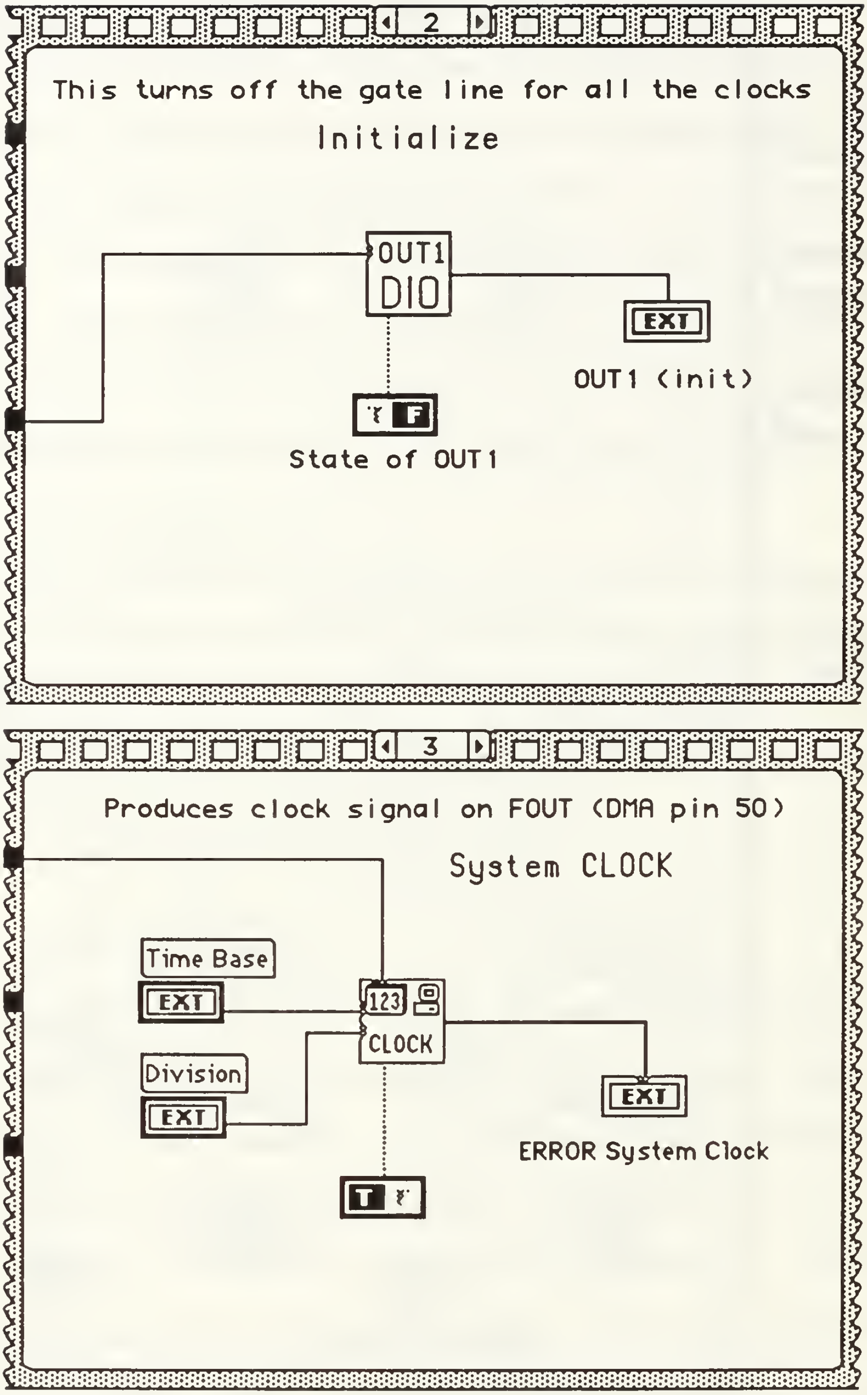


Figure 5-16 Telemetry Clocks VI Block Diagram (Frames 2 and 3)

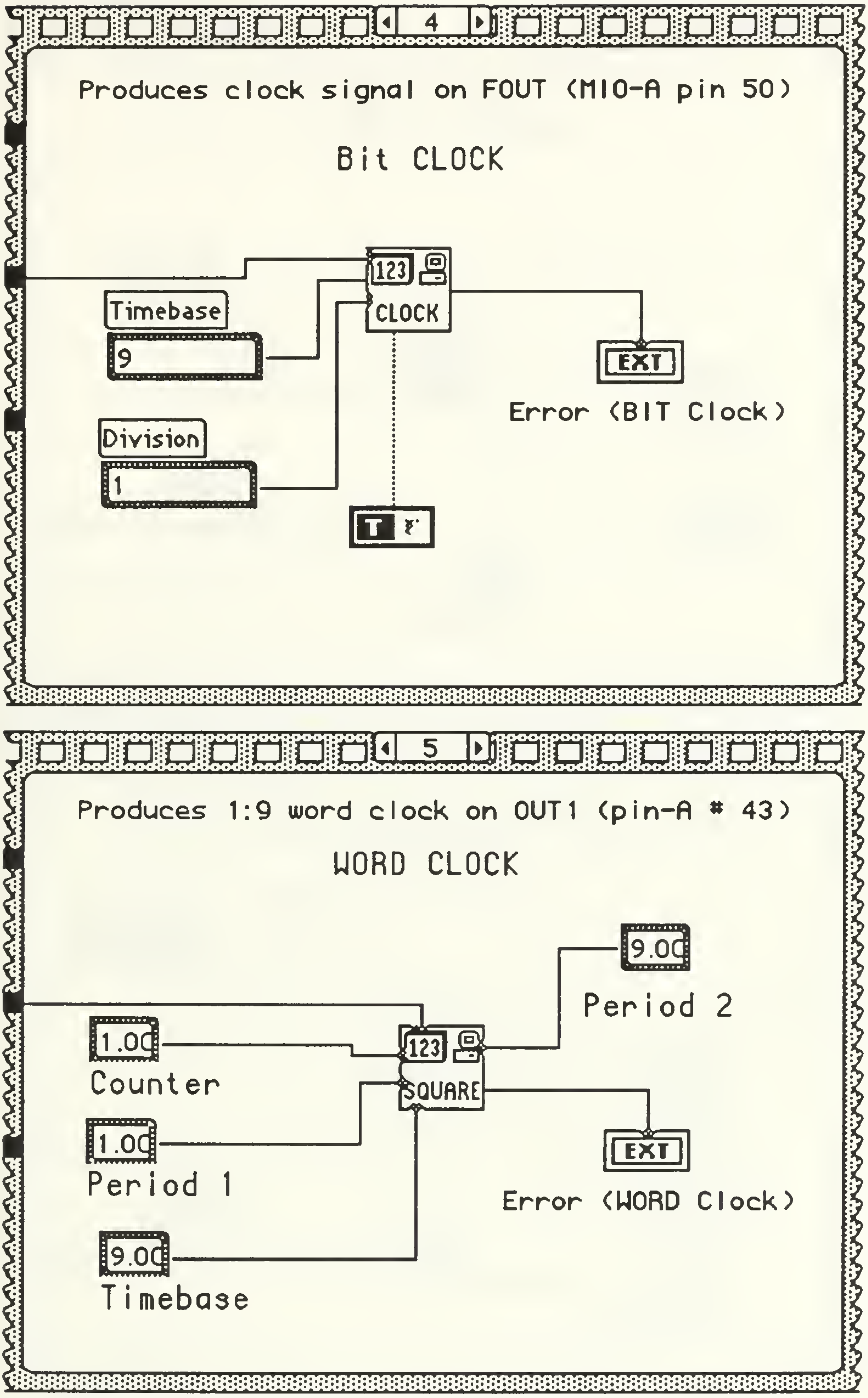


Figure 5-17 Telemetry Clocks VI Block Diagram (Frames 4 and 5)

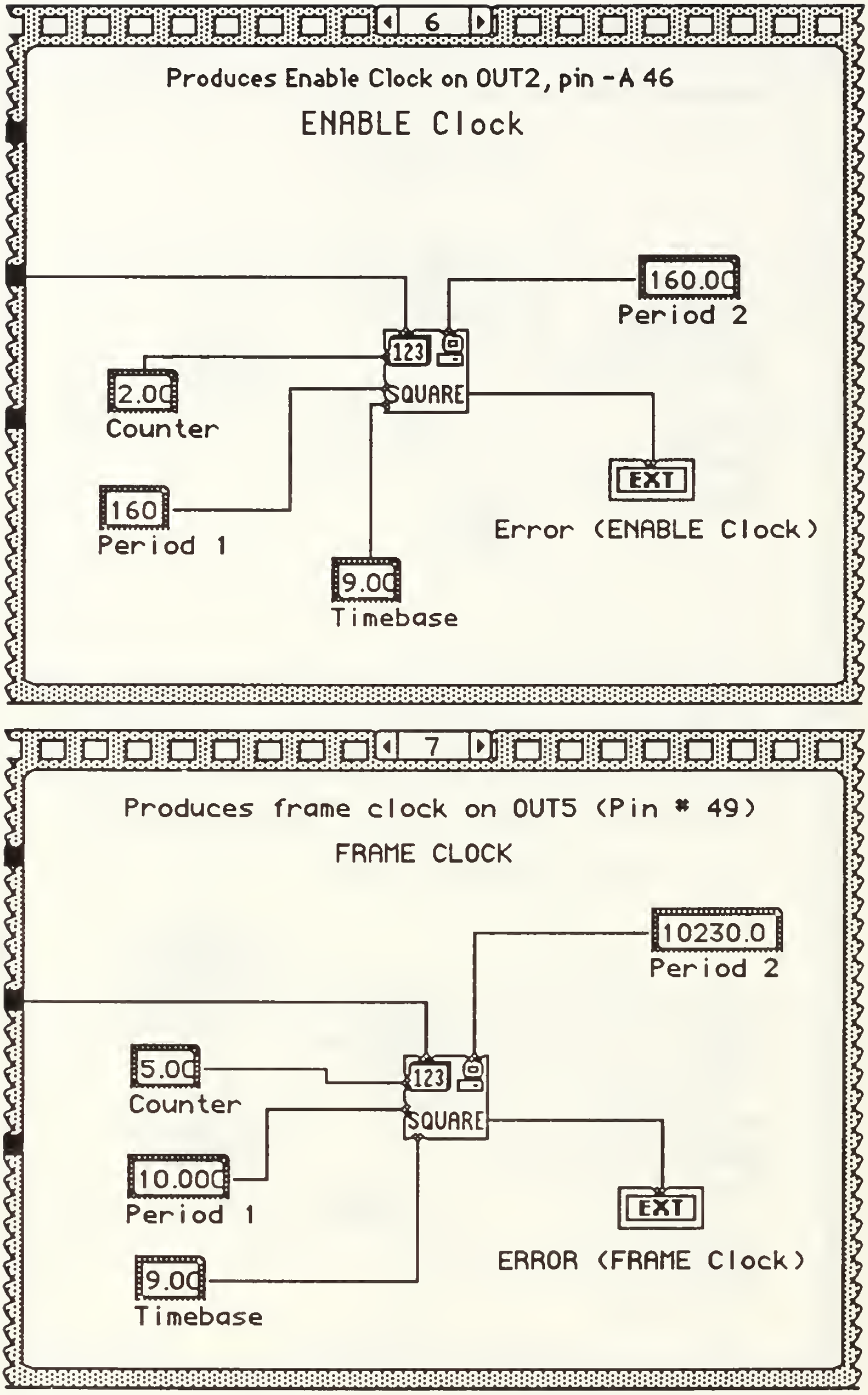


Figure 5-18 Telemetry Clocks VI Block Diagram (Frames 6 and 7)

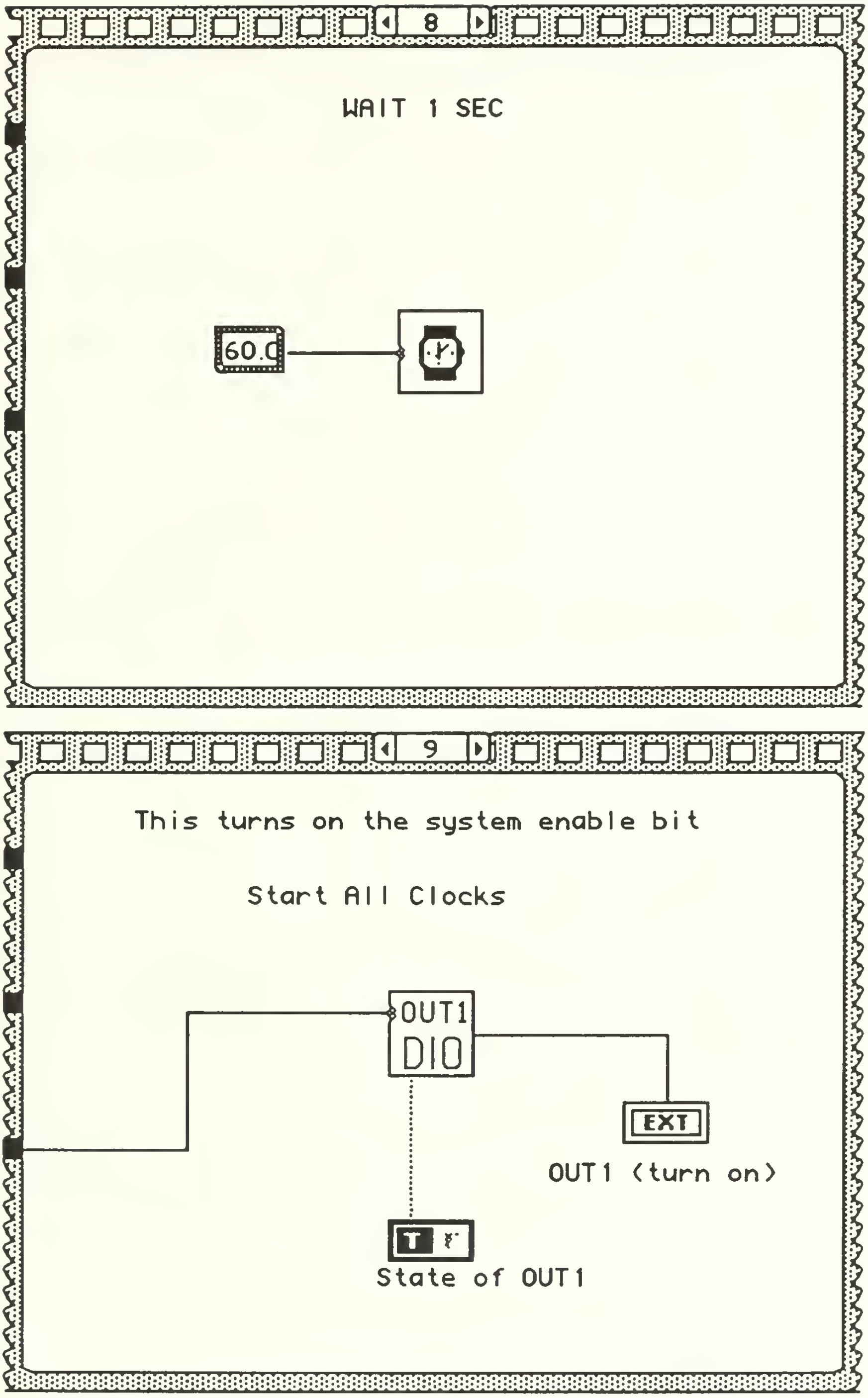


Figure 5-19 Telemetry Clocks VI Block Diagram (Frames 8 and 9)

- DMA board is to be configured
- Signal code zero (FOUT) of the DMA board is assigned to the bus
- FOUT signal is placed on trigger line zero of the RTSI bus
- DMA board is the source of this signal (DMA board transmits)
- MIO board is to be configured
- Signal code four (SOURCE4) of the MIO board is assigned to the bus
- SOURCE4 is assigned to the same trigger line zero as FOUT above
- MIO board is the destination of the signal (MIO board receives)

The sub-VI, OUT1 of DIO, is called in frame two, and its operation is discussed in the next section of this chapter. It places a digital line in a logic low level. This digital line is referred to as the GATE in the GSE interface circuit, and its function is to ensure that all the clocks are synchronized to start at the same time. This GATE line is wired to the external gate input of all of the clocks. Frame three calls the *CTR_Clock* LabDriver VI. This frame starts the master system clock running on the DMA board as follows.

- DMA board in NuBus slot #2
- Timebase set to internal 1MHz clock by entering a one on the front panel
- Division by five on the front panel results in a 200kHz clock
- Output signal frequency is enabled

Frame four produces the Bit Clock at pin 50 of the MIO connector by calling the same LabDriver VI. The MIO board receives the system clock as an input, and sends it out unaltered as the Bit Clock.

- MIO board in NuBus slot #3
- Timebase set to external SOURCE4 line on the MIO board. This means that the MIO board is receiving the master system clock from the DMA board via this line of the RTSI bus.
- Division by one results in a 200kHz clock for the Bit Clock
- Output signal frequency is enabled

Frame five produces the Word Clock at pin 43 of the MIO connector by calling the *CTR_Square* LabDriver VI. This library VI allows the output of a square wave signal which has a duty cycle other than 50 percent, which is necessary for the other telemetry clocks. The Word Clock is constructed from the master system clock as follows.

- MIO board in NuBus slot #3
- Counter one of the MIO board is used for the Word Clock
- Timebase also set to external SOURCE4 line on the MIO board
- Period one is set to one. This means that the on-cycle of the square wave will be equal to one period of the timebase.
- Period two is set to nine. This means that the off-cycle of the square wave will be equal to nine periods of the timebase.

Frames six and seven produce the Enable Clock at pin 46 and the Frame Clock at pin 49 of the MIO connector in the same fashion. The *CTR_Square* LabDriver VI is also used here. These clocks, described at the beginning of this chapter, are constructed as follows.

- MIO board in NuBus slot #3
- Counter two of the MIO board is used for the Word Clock
- Counter five of the MIO board is used for the Frame Clock
- Timebase for both is set to external SOURCE4 line on the MIO board
- Period one of the Word Clock is set to 160 periods of the timebase
- Period two of the Word Clock is set to 160 periods of the timebase
- Period one of the Frame Clock is set to 10 periods of the timebase
- Period two of the Frame Clock is set to 10230 periods of the timebase

Frame eight inserts a one second pause before the clocks are started. Frame nine asserts the GATE line by calling the OUT1 of DIO VI after the one second delay. When the GATE line goes high, all clock timers are enabled, and they all begin in a synchronized fashion.

The OUT1 of DIO sub-VI is called in the Telemetry Clocks VI, and its simple block diagram is shown in Figure 5-20. The *DIG_Out_Line* LabDriver VI is called in this block diagram. This VI configures one digital line on the DIO board to act as the GATE signal for gating of all of the clocks. The DIO board in NuBus slot #4 is selected. Port #4 of the DIO board is the location of the port where the digital line will be used. This is a special port and consists of three permanent input lines and three permanent output lines. Line #0 is selected which corresponds to the OUT1 line. This is pin 31 of the DIO connector shown in Figure 5-13. The state input controls whether the OUT1 line is in a logic high or logic low state. Frame two of the Telemetry Clocks VI turns the GATE signal off, and frame nine turns it on.

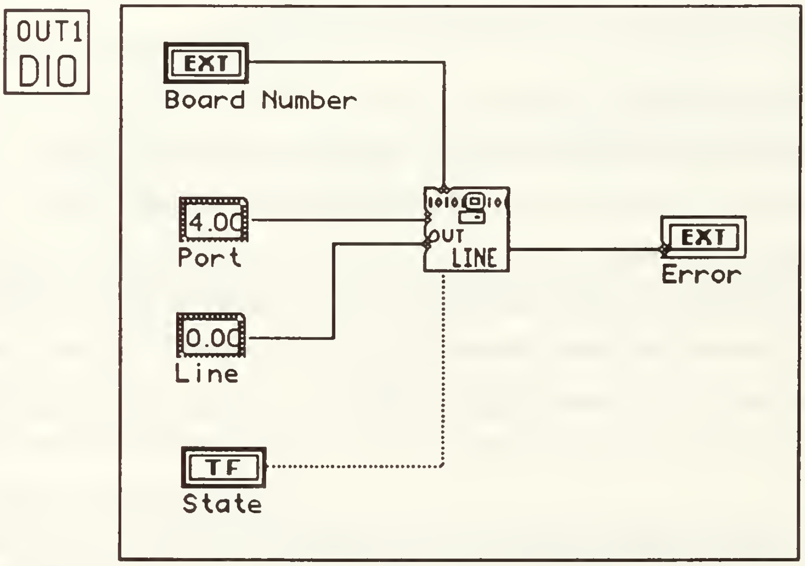


Figure 5-20 OUT1 of DIO Board VI Block Diagram

d. Data Acquisition

Once the NI data acquisition boards have been initialized and the telemetry clocks are running, MUSTANG data may be acquired by clicking the Data Acquisition button of the Main GSE VI. This launches the Data Acquisition sub-VI. The front panel window was shown in Figure 5-6, and the block diagram is shown in Figures 5-21 and 5-22. The front panel window of the Data Acquisition VI automatically opens when the sub-VI is called. This does not happen for any of the other sub-VIs. Normally a sub-VI is called, executed and control is then returned to the calling VI. The calling VI has its front panel showing the entire time. This feature can be configured by command-clicking on the Data Acquisition icon in the front panel window. Select *VI Setup* from the pop-up menu. Under the *When used as a sub-VI from any node:*, select the options *Show front panel when called* and *Close afterwards if originally closed.* This will allow the Data Acquisition graph display in its front window to come into view when the VI is called from the Main GSE VI.

It is very important that power be applied to the MUSTANG instrument prior to clicking the Data Acquisition button. The power is necessary in order for the MUSTANG circuit to return the proper handshaking signal. If the MUSTANG is not powered, the handshaking signal will not be produced, and the VI will wait for the signals in an endless loop. To recover from this, the *DIG_Blk_Clear* LabDriver VI had to be executed to clear the digital input group prior to proceeding. To correct for this inconvenience, the *DIG_Blk_Clear* VI was added to the Data Acquisition VI so that it is executed every time the VI is entered to automatically clear the input group. The *DIG_Blk_Clear* VI has no output, but is wired to the while loop structure. This illustrates the artificial data

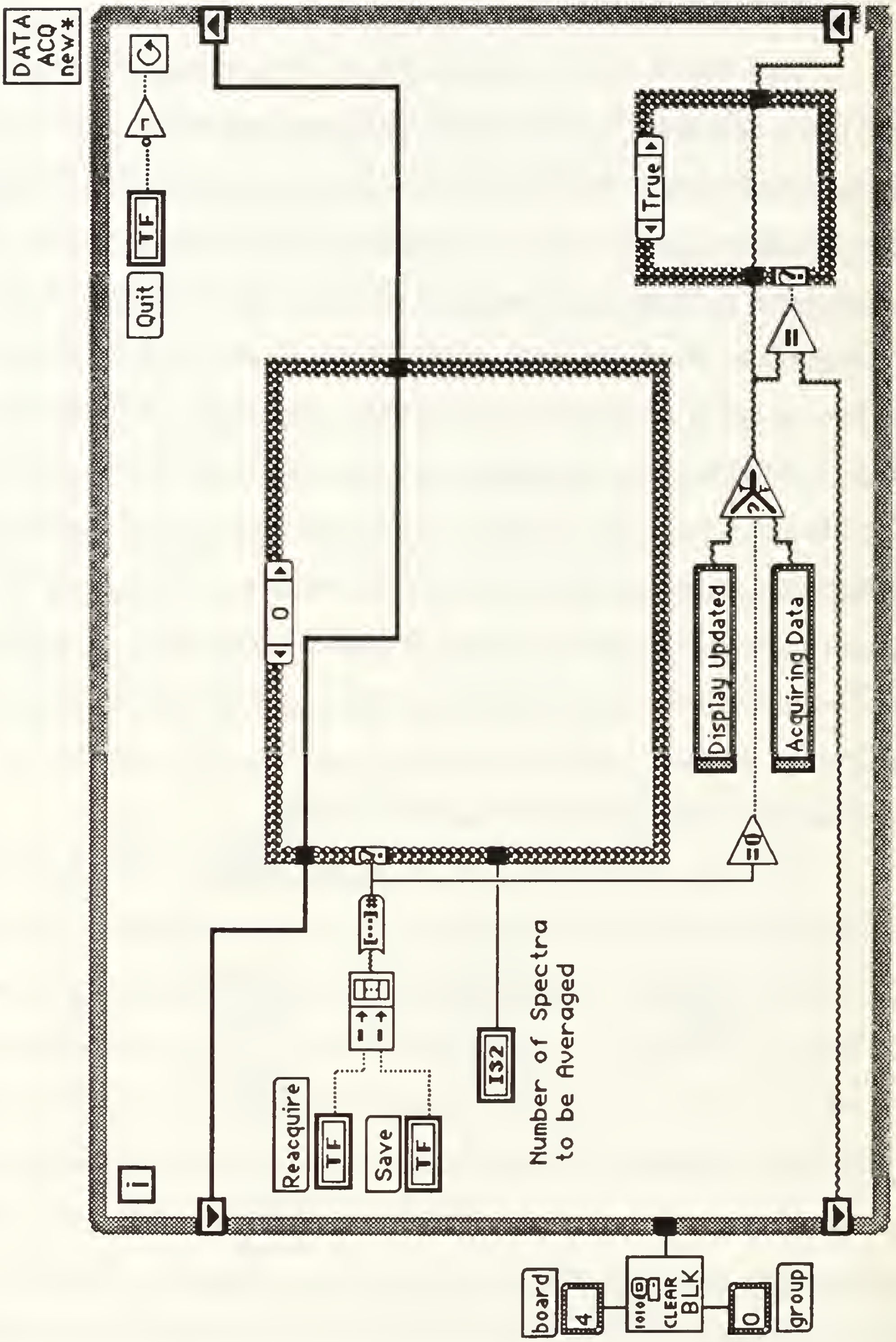


Figure 5-21 Data Acquisition VI Block Diagram

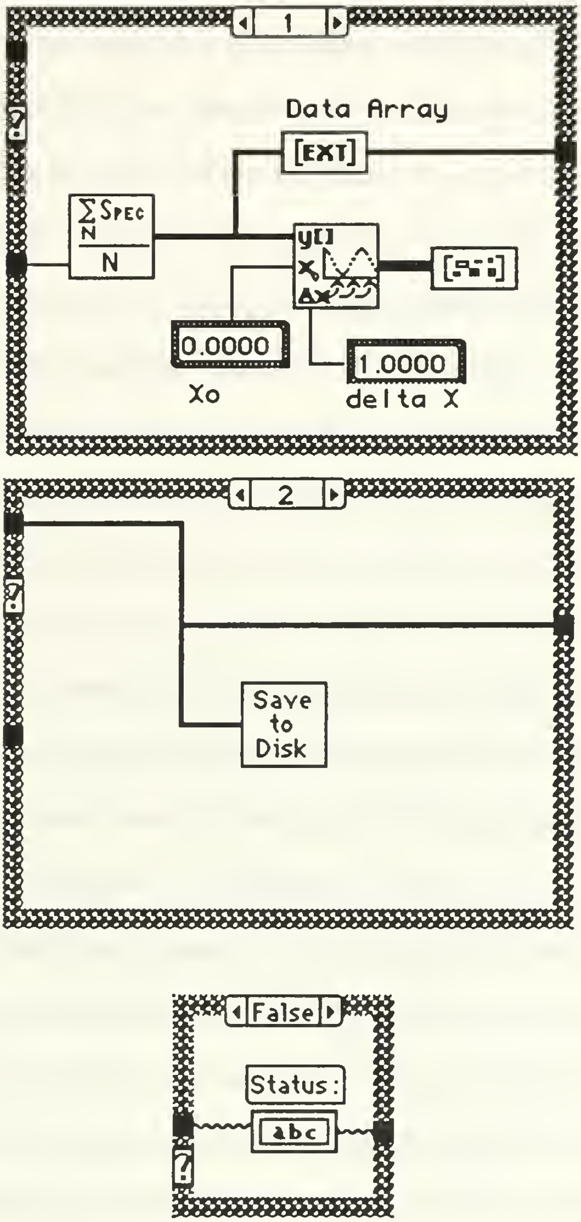


Figure 5-22 Data Acquisition VI Block Diagram Subsequent Cases

dependency capability of the LabVIEW program. The VI which clears the input group will execute prior to entering the while loop.

The Data Acquisition program is contained within a while loop with two shift registers. The top shift register holds the MUSTANG spectrum that is acquired, which consists of an array of 512 pixel values. The lower shift register holds the status message displayed at the bottom of the Data Acquisition front panel window. The quit button is again wired through an inverter to the while loop conditional terminal. The iteration terminal is not used for anything in this block diagram. The other two front panel buttons for Reacquiring a spectrum and Saving it to disk are bundled into a boolean array and converted to a decimal number. This is done the same way as was done in the Main GSE block diagram.

When no button is clicked, then case zero is selected, and the 512 values in the spectrum are cycled through the shift resister. A zero is also sent to the *Equal to Zero* comparator. The comparator output is a boolean TRUE which causes the top input to the *Select* function to be passed to the second case structure. The first time the program is run, this is not equal to the null string in the shift register so the False case is selected and the status window is updated with the Display Updated message. Despite this message, there is really no spectrum displayed until the user clicks the Reacquire button the first time. On the next iteration of the while loop, the *Equality* comparator sends a boolean TRUE to the case structure to select the true case, and the status window is not updated, thus preventing the flickering message on the screen as before.

When the Reacquire button is clicked, case one is selected. This calls the sub-VI to acquire a new spectrum, and sends the spectrum values to the

Array to Graph function. This function sends the array values to the graph on the front panel window. While the reacquire button is depressed, the value of the boolean array is not zero. This causes a boolean FALSE to be sent out of the *Equal to Zero* comparator, and the Acquiring Data message is selected by the *Select* function. This value is different from the text string stored in the shift register, so the output of the next *Equality* function selects the false case in the second case structure. This updates the status window with the new message, Acquiring Data. The new spectrum is obtained and plotted, and the next iteration of the while loop continues. Now, there are no buttons depressed, so the Display Updated message is sent to the status window. This lets the user know when the program is at work collecting the next spectrum, and when the display on the screen has been updated. This is convenient when many spectra are acquired and averaged. One of the inputs on the Data Acquisition VI front panel is for the number of spectra to be averaged. If this number is on the order of 50, it can take approximately four seconds for all of the data to be taken before the display is updated.

When the Save button is clicked, case two is selected in the first case structure. This case calls the Save to Disk sub-VI, which stores the current array to disk as explained in a later section. This case also causes the status window to be updated as if a new spectrum is being acquired. No new data is actually taken. This was just the easiest way to construct the block diagram. When the status window updates with the Display Updated message, it really only means that the save operation is complete.

The actual work done in collecting the data for the new spectrum is done in the Average N Spectra VI which is called in case one. The operation of this sub-VI is described in the next section.

(1) Average N Spectra. This VI uses the sequence structure with three frames in its block diagram illustrated in Figures 5-23 through 5-25. The number of spectra to be averaged from the front panel is passed into the sequence structure. A sub-VI, Get N Spectra, is called in frame zero. This VI actually collects the data for the number of spectra specified by the user. The data collected is in one long array which is passed to the subsequent frames via a local variable indicator. The function of the Average N Spectra VI is to average the number of spectra obtained, and return one spectrum of 512 pixel values. The output data array is initialized to zero in frame zero, and passed to subsequent frames via another local variable indicator.

Frame one contains the For loop structure. The limit for the for loop operation is set by wiring the number of spectra to be averaged to the count terminal. The iteration terminal holds the value of the current iteration of the for loop from zero to N-1. A shift register is used in the for loop to pass the current value of the output data array to the next iteration. The long data array which holds all of the spectra to be averaged is passed into the for loop from the upper local variable terminal. This array is sent into an *Array Subset* function. The index for the array subset is equal to 512 times the current iteration of the for loop. The length of the array subset is 512, or the length of one spectrum. The output of the *Array Subset* function is an array with 512 elements which is taken from an integer number of spectra into the acquired data array. This single spectrum is wired to the *Addition* function where it is added to a running

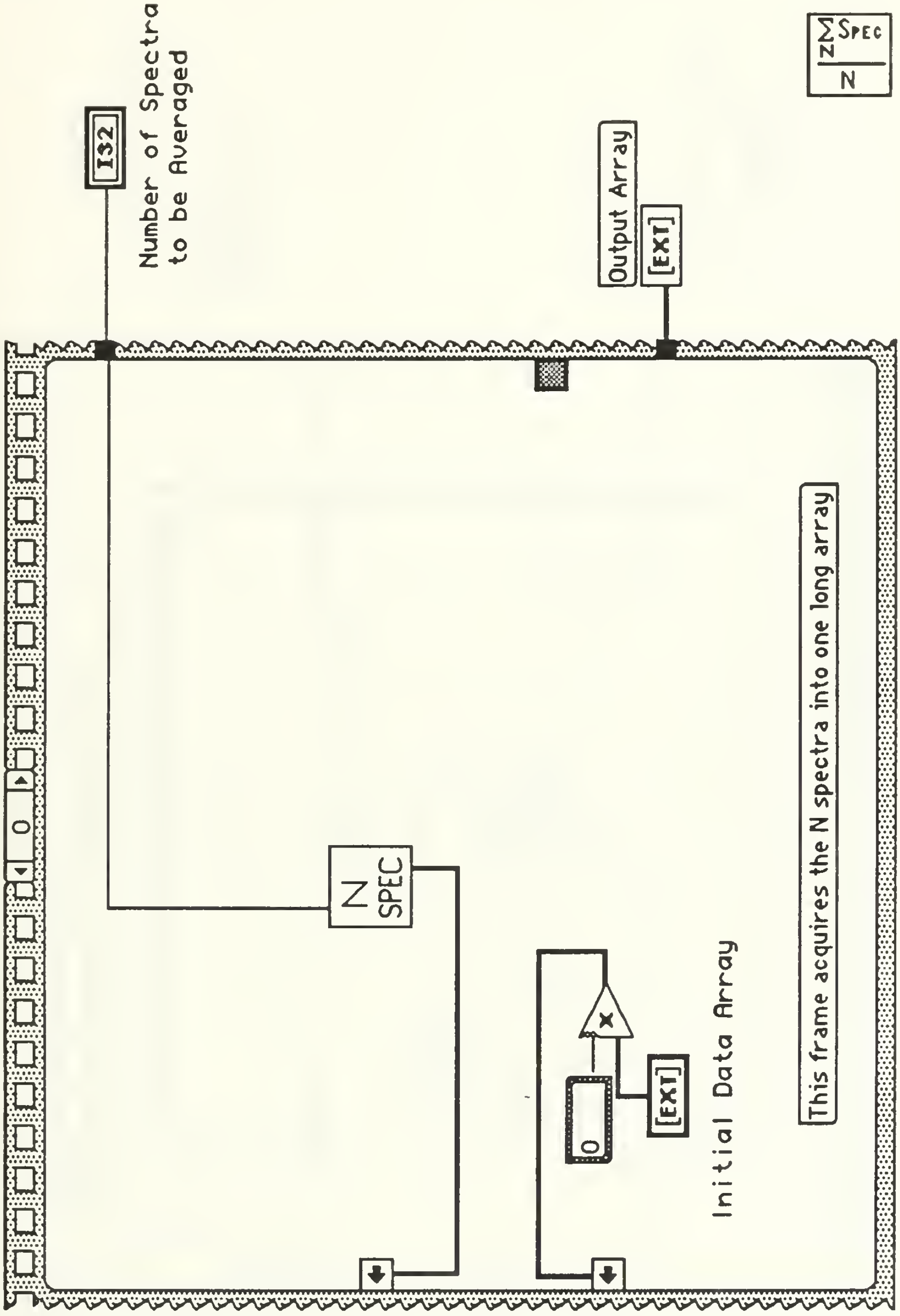


Figure 5-23 Average N Spectra VI Block Diagram (frame 0)

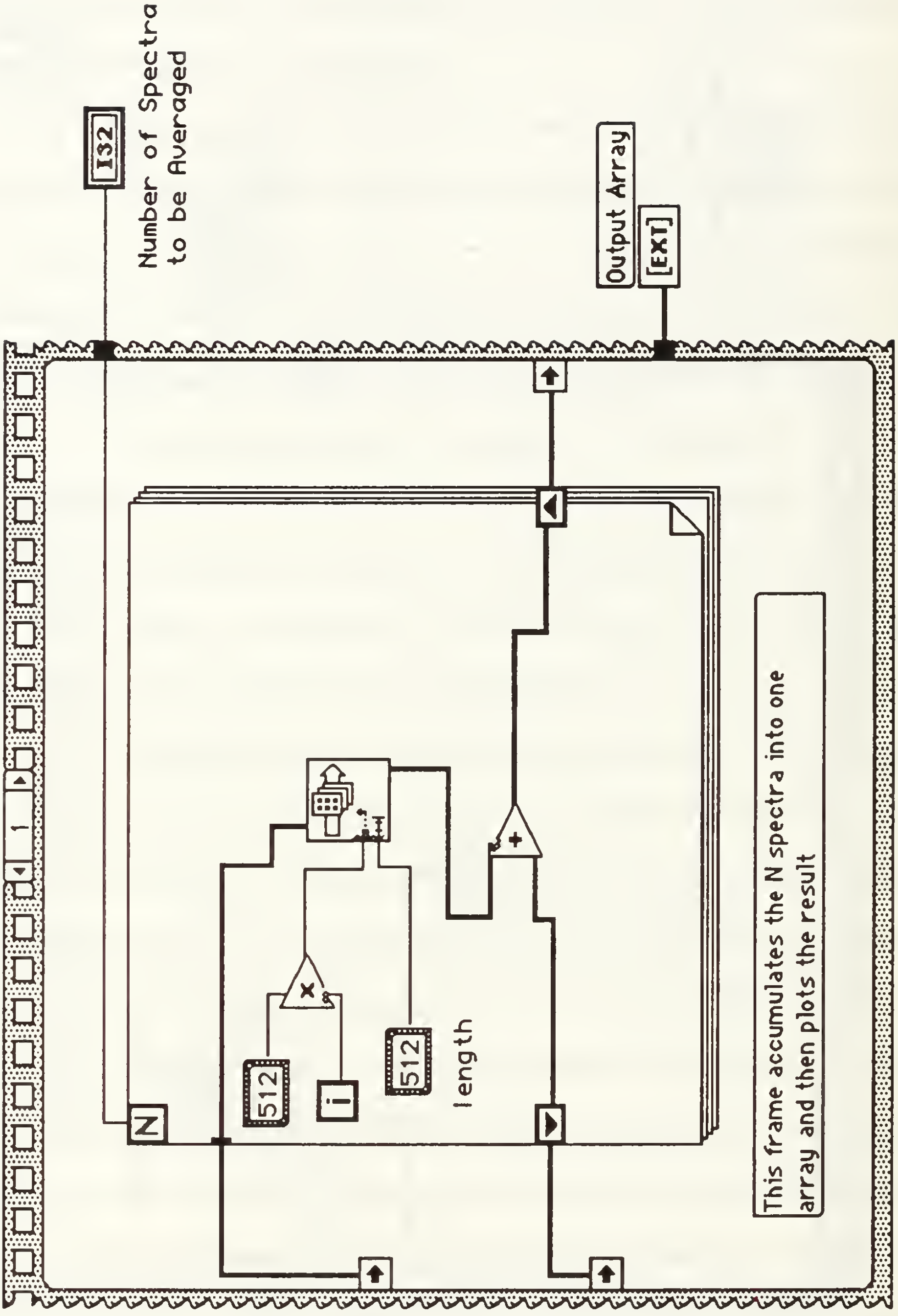

I32
Number of Spectra
to be Averaged
Output Array
[EXT]
1
N
512
i
512
length
This frame accumulates the N spectra into one
array and then plots the result

Figure 5-24 Average N Spectra VI Block Diagram (frame 1)

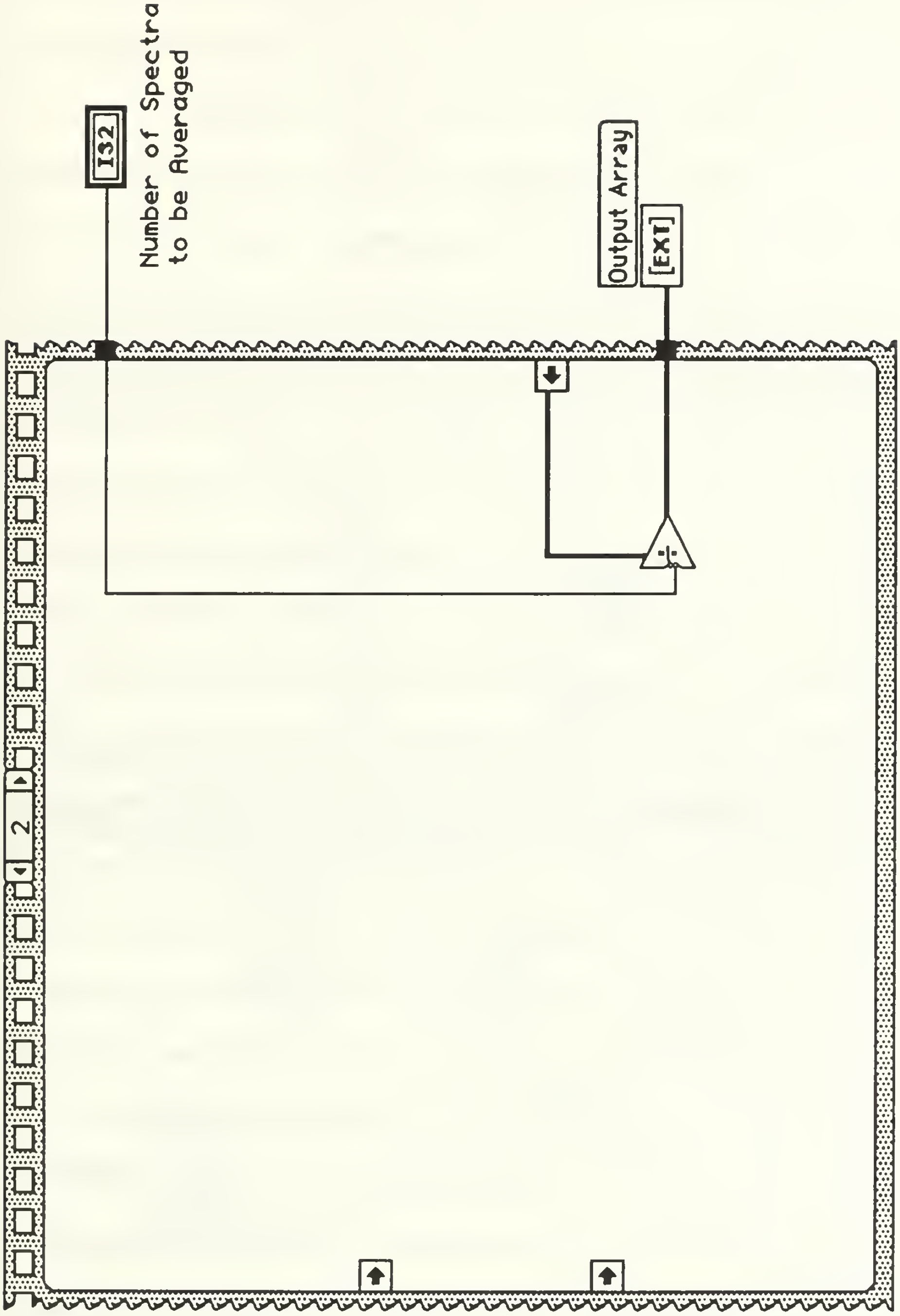


Figure 5-25 Average N Spectra VI Block Diagram (frame 2)

total in the output array as the for loop progresses. The first time through, the spectrum is added to zero since the output array was initialized to zero. When the for loop completes, all of the N spectra acquired have been added up, and the result is passed to the next frame via another local variable.

Frame two actually performs the averaging process. The summed output array is divided by the number of spectra to be averaged. The value of the averaged spectrum is passed back to the calling VI which was Data Acquisition.

(2) Get N Spectra. This sub-VI, called in frame zero of the Average N Spectra VI, is finally the one which collects the MUSTANG data on the digital input port lines. It has been significantly revised from past versions of the program. Several VIs are now incorporated into this one VI with a sequence structure. All three frames of the sequence in the block diagram are shown in Figure 5-26. The first two frames call the *DIG_Out_Line* LabDriver VI which was also used in the OUT1 of DIO VI. These frames configure one digital line on the DIO board as the SWITCH signal which is used to trigger the GSE interface hardware described in a later section. The DIO board in NuBus slot #4 is selected. The special port #4 of the DIO board is again selected as the source of the digital output line. Line #1 is selected this time, which corresponds to the OUT2 line. This is pin 22 of the DIO connector shown in Figure 5-13. Frame zero sets the state of the digital output line to a logic low level. Frame one resets the output line to a logic high level. The SWITCH line in the external hardware needs a rising edge in order to start the data collection at the beginning of a spectrum. This transition of the OUT2 line of the DIO board provides this

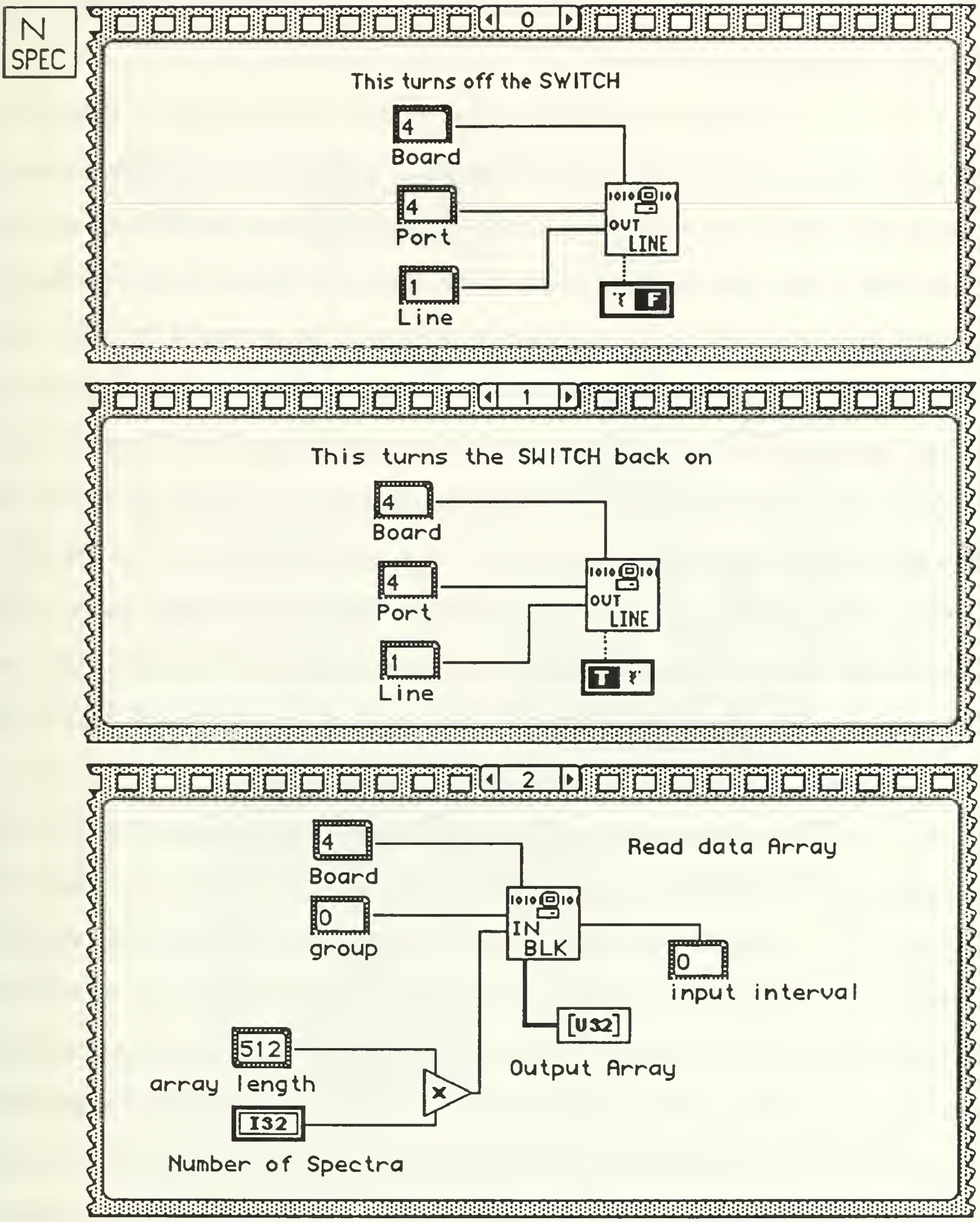


Figure 5-26 Acquire N Spectra VI Block Diagram

rising edge to ensure that the first pixel obtained corresponds to pixel one of the MUSTANG spectrum.

Frame two calls the *DIG_Blk_In* LabDriver VI. This is the VI which latches in the data. The DIO board in NuBus slot #4 is again selected. Group zero which was configured as the input group when the I/O boards were initialized, is also selected. The count of the number of digital words to collect is created from multiplying the number of spectra to be averaged by 512. The collection interval is set to zero since the data is latched via a handshaking signal. When frame two begins execution, the REQ1 signal on pin 33 of Figure 5-13 is monitored for a handshake signal. Each handshake pulse which appears on this line causes a new data word to be latched. The data is physically collected into a buffer in the computer memory which is represented by the output array. This is one long array with length equal to an integer multiple of 512, depending on the number of spectra to be averaged. This long data array is passed back to the calling VI described previously which averages the spectra.

(3) Save to Disk. This sub-VI is called in case two of the Data Acquisition VI. Its block diagram uses the For loop structure and is shown in Figure 5-27. This VI has been totally rewritten from the previous version. Artificial data dependency is used to control the program flow. A new file is first opened with the *New File* function which is wired to the for loop boundary. No data is passed to the for loop on this wire. The wiring ensures that the new file will be opened before the for loop is executed, and data is written to the file. The same technique is used to close the file. The for loop must complete operation prior to calling the *Close File* function.

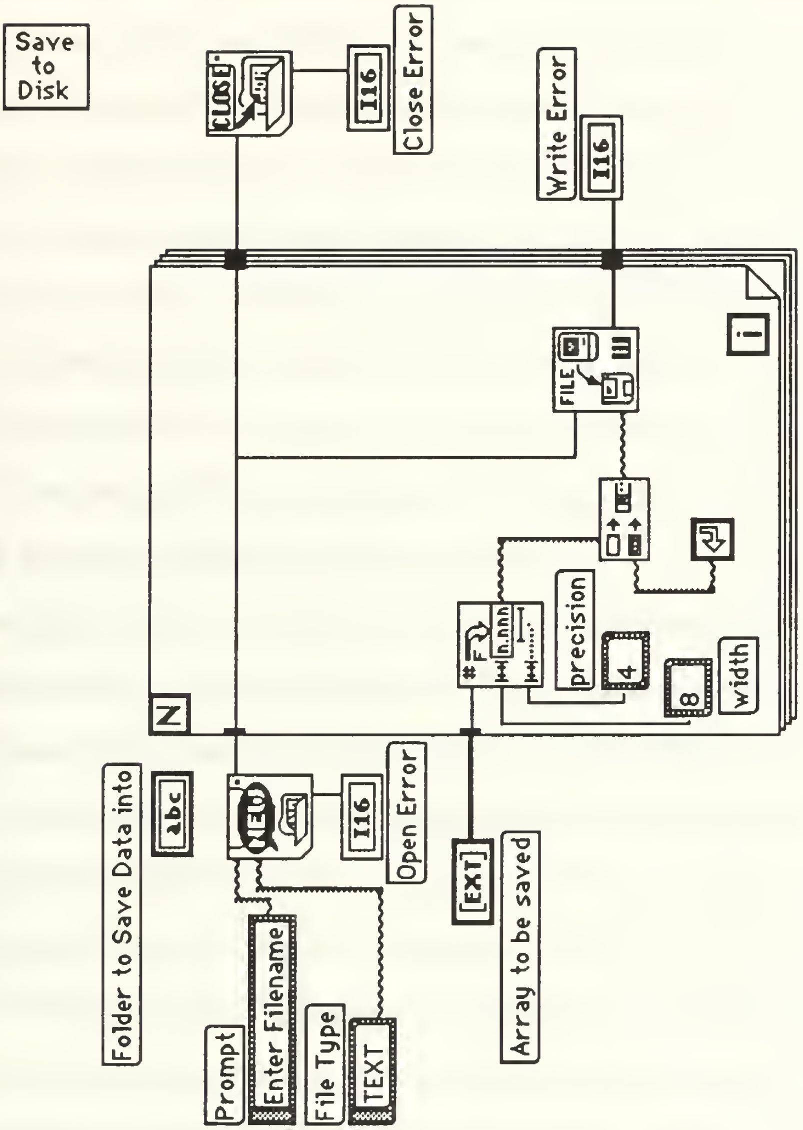


Figure 5-27 Save to Disk VI Block Diagram

The *Open File* function brings up the standard Macintosh open file dialog box when executed. The prompt string can be entered, and will be displayed in the dialog box to tell the user what to type in for a filename. The file type must be entered, and the standard TEXT file is used in this application. A LabVIEW file type could have been used in order to allow for recalling the spectrum later, and displaying it on the LavVIEW graph. Most of the MUSTANG data is analyzed on a separate Digital VAX computer system, so the TEXT file is a good standard to use when transferring data between computers.

The For loop writes the data to the previously opened file. There is no input to the For loop count terminal, so it utilizes an auto-indexing mode. The indexing occurs on the loop boundary. The array sent into the for loop has 512 elements, so the For loop will execute 512 times, and bring in one element of the array with each iteration. An array can also be created on a loop boundary by the same principle, but this feature is not used in this VI. The number sent into the for loop from the array is a floating point number and must be converted to a string for storage in a text file. The array element is sent into the *To Fractional* function. The output is an eight character floating point string with precision to four decimal places. A carriage return is appended to the element and it is written to the file. File pointers are maintained within the LabVIEW program so the user need not be concerned with where the value is being written in the file. The completed TEXT file has 512 lines of data with one floating point number per line. After the last array element has been written to the file, the file is closed, and control is returned to the calling VI.

3. Launch Software

The program described above must be changed when used to monitor the MUSTANG in the launch configuration. When the instrument is in the rocket, a separate GSE electronic interface box is used. This interface has no connection between the GATE signal out of the DIO board and the gate inputs to the counters on the MIO board. The lab GSE interface makes this connection inside the box. In the launch configuration, the software is changed to provide the GATE signal out of the MIO board at BDIO3, pin 32 in Figure 5-1. When the Launch GSE interface is used, a connector adapter is used to connect the MIO cable to the T/M input. This adapter connects the GATE signal at pin 32 to the gate inputs for the counters at pins 42, 45 and 48 of Figure 5-1.

a. Launch Telemetry Clocks

The software modification for the launch configuration is shown in Figures 5-28 and 5-29. Only two frames of the Telemetry Clocks VI need to be changed. These frames call the OUT3 of MIO sub-VI which controls the BDIO3 output line of the MIO board. The only purpose of this change in the software is to synchronize the telemetry clocks when using the Launch GSE interface. The data is still acquired as described previously.

A separate sub-VI, called Launch Clocks, which has these changes has been written for use with the Launch GSE. It can easily be placed in the Main GSE VI by command clicking on the Telemetry Clocks VI icon in Figure 5-10 and choosing *Replace VI* from the pop-up menu. This one simple software change is all that is necessary to shift from the Lab to the Launch GSE configuration.

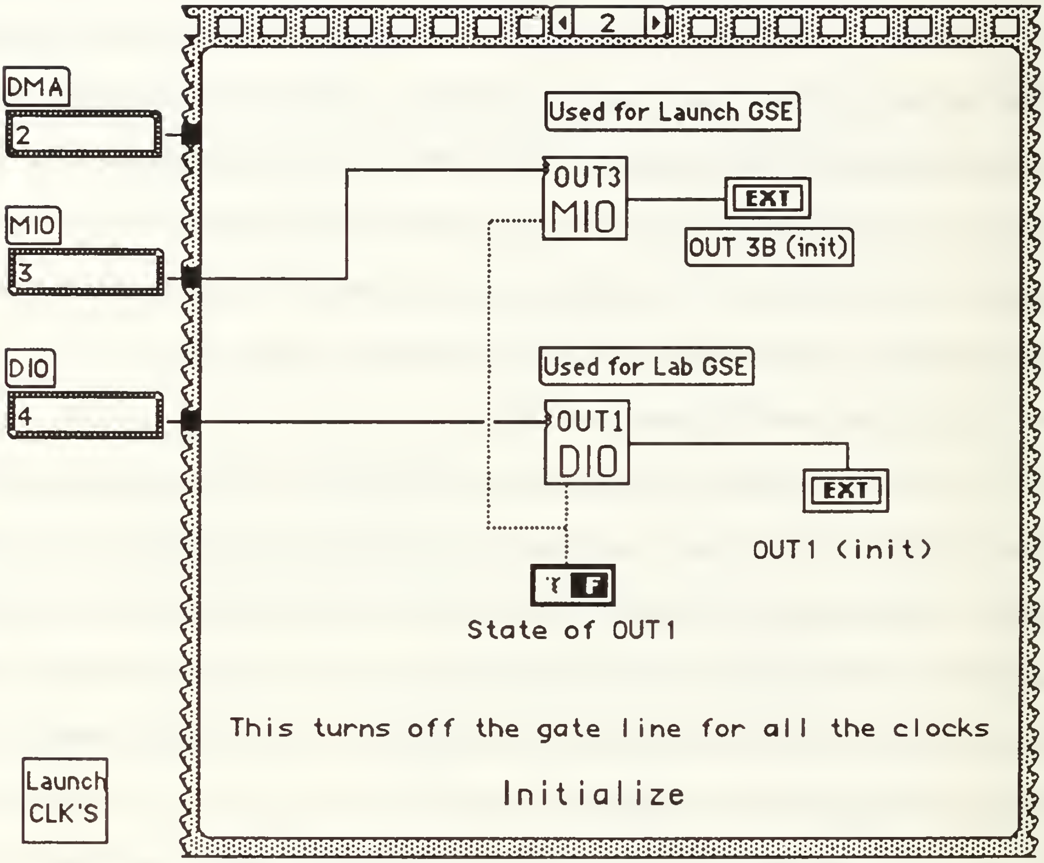


Figure 5-28 Launch Telemetry Clocks VI Block Diagram (frame 2)

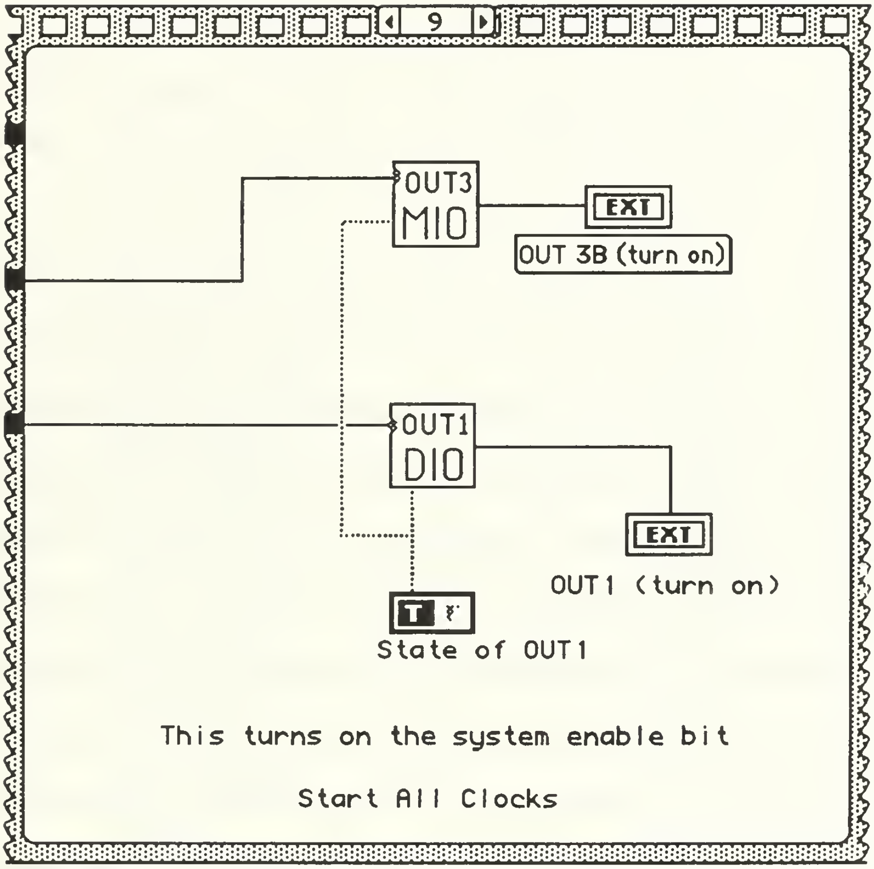


Figure 5-29 Launch Telemetry Clocks VI Block Diagram (frame 9)

b. Faulty Telemetry Clocks

An attempt was made to create a faulty set of telemetry clocks in the LabVIEW program which would simulate the overlapping Enable Clock shown in Figure 2-5. If the GSE clocks could be made to look exactly like the real telemetry clocks, then there would be no uncertainty about the interface circuit operation in the launch configuration.

The system clock is formed by using an internal 1MHz clock as a timebase, and dividing it by five to get the 200kHz clock. In order to get the small overlap in the Enable Clock with the 17th Word Clock pulse, it is necessary to have a much finer time unit than 5µs. The clocks can be constructed directly from the 1MHz internal clock, which gives a time unit of 1µs. Using this clock for the master system clock would theoretically enable construction of an Enable Clock which is similar to the real waveform. Unfortunately, when using a time unit this small, a limitation in the software is reached. This limitation is described in Reference 8, and occurs when using the high clock speeds as a timebase for the counters. It becomes impossible to predict if the counter will synchronize to the timebase in the first period, or if it will require an additional period to synchronize. This uncertainty makes it impossible to synchronize all of the telemetry clocks in this application when using the fastest timebase.

This problem appears to be an inherent limitation in the LabVIEW software, and an alternate solution is not immediately apparent. The above method was tried and the clocks were found to be synchronized differently each time the program was run.

TABLE 5-2 LABDRIVER LIBRARY VIs

LabDriver VI	**Reference 8 page number**
DIG_Prt_Config	4-7
DIG_Out_Line	4-10
DIG_Grp_Config	4-14
DIG_Grp_Mode	4-16
DIG_Blk_In	4-21
DIG_Blk_Clear	4-26
CTR_Config	6-9
CTR_Square	6-23
CTR_Clock	6-25
RTSI_Conn	7-7
RTSI_Clear	7-10

C. GSE HARDWARE EQUIPMENT

The two GSE electronic interface boxes synchronize the collection of the MUSTANG data the same way. The interface is responsible for sending the handshaking signals to the MIO board, and for synchronizing the first handshake signal with the first pixel read out in the frame. The circuit diagram for the GSE interface electronics is shown in Figure 5-30. While this diagram may not match up pin-for-pin with the existing circuit, it is functionally correct. Figure 5-31 is the timing diagram which shows the control waveforms for the GSE interface electronics.

The Latch signal is used from the MUSTANG interface as a trigger signal for generation of the handshake pulse. The Latch is fed into the input of the first monostable multivibrator, which is programmed to generate a 10.4μs positive pulse on the falling edge of Latch. This pulse is fed into the input of the second monostable on the same chip which generates a 5.2μs positive pulse with the rising edge of the input. I would have expected this pulse to be generated on the falling edge of the 10.4μs pulse. That would have effectively inserted a 10μs delay in collecting the data. In the current configuration, the 10.4μs pulse serves no purpose, and is not used. In any case this delay is critical to the proper collection of data from the MUSTANG.

The 5.2μs positive pulse is sent to an And gate which forms the handshake signal. The other input to the And gate is the output of the D-flip-flop. The flip-flop is clocked by the Frame Clock, and is rising-edge triggered. When the Data Acquisition VI is called in the program, the SWITCH signal is set low and then high by the OUT2 of DIO sub-VI. The SWITCH is on pin 22 of the DIO connector shown in Figure 5-13. The low-to-high transition of this signal

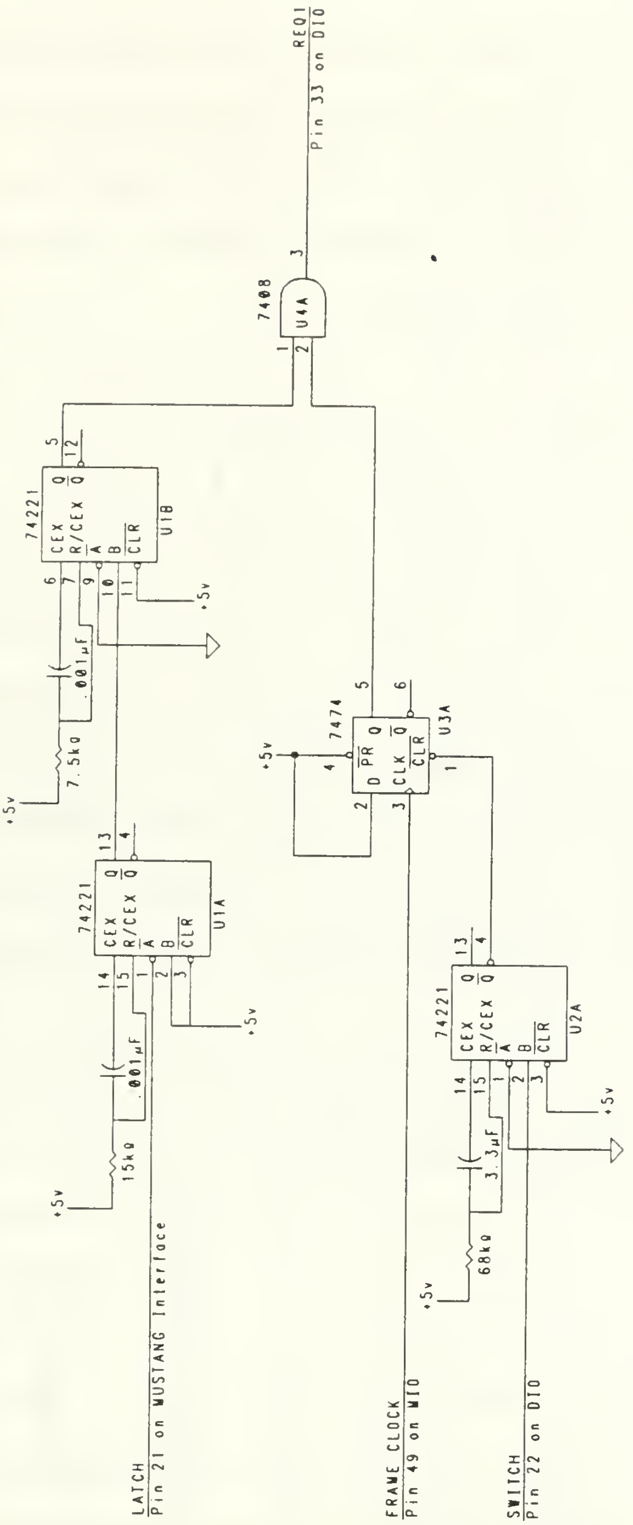


Figure 5-30 GSE Interface Electronics Circuit Diagram

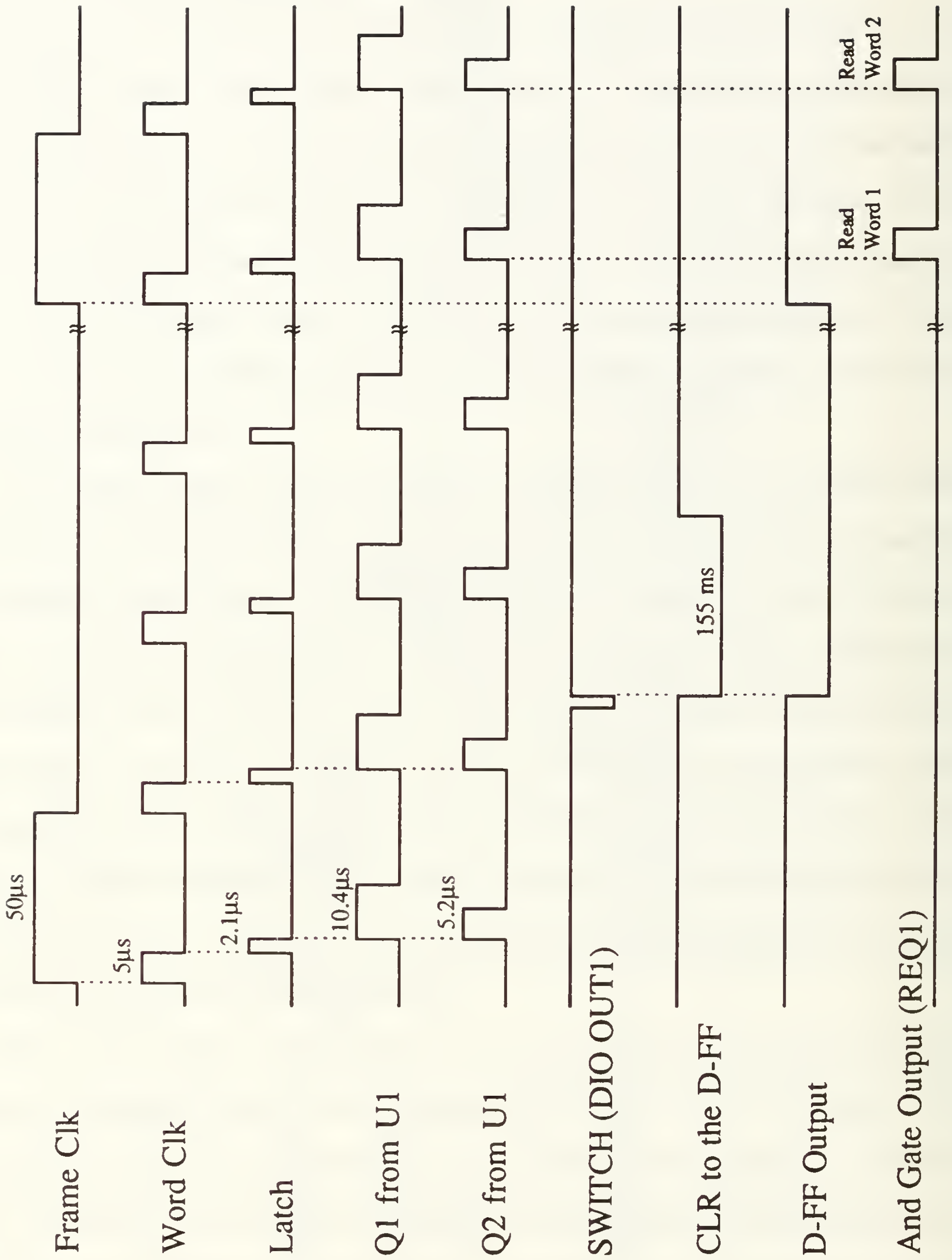


Figure 5-31 GSE Interface Electronics Timing Diagram

triggers a second monostable which produces a negative pulse that is the Clear input to the D flip-flop. Since the flip-flop has an asynchronous clear input, its output goes low immediately, and does not go high again until the next Frame Clock pulse. After the next Frame Clock pulse, the flip-flop sends a logic high level to the And gate. The And gate output will then be equivalent to the monostable pulses at its other input.

The key to getting this configuration to acquire data in a synchronous manner is for the LabVIEW program to be ready to start latching data when the first handshake pulse occurs. The time delay between the time the LabVIEW program is executed and the time when it is really ready to accept data at the DIO ports is not documented in the manuals. Experience has shown that several frames of data can go by before data is actually collected. This amounts to several hundreds of milliseconds which is not unreasonable, but it was also not accounted for in the original design of the GSE interfaces. The duration of the monostable pulse that is the flip-flop clear is the critical parameter in making this interface work.

One frame of MUSTANG data is taken in 51.2ms. The flip-flop Clear signal was originally set to have a duration of 31ms which is less than one frame. The duration was adjusted to the maximum possible value of 155ms without exceeding the maximum resistor value for the monostable. This pulse can be lengthened further by adding an additional capacitor in parallel. This modification to both the Lab and the Launch GSE interfaces improved the reliability of data synchronization considerably, but it is still not flawless.

Additional modifications were also made to the GSE interface boxes in preparation for the next MUSTANG launch. Both boxes had to be modified to accommodate the additional -15V signal for the high voltage circuit which was added with the new interface circuit. Both boxes also had to be modified to use the Gain Select signal which was added for the next launch. A mechanical switch was added on the Lab GSE interface box to allow the user to select the desired gain for testing and calibration. In the Launch GSE interface box, the Gain Select signal comes from telemetry, and must be monitored in software.

D. SPARE DETECTOR BOX CONSTRUCTION

A method of testing the MUSTANG interface without actually having to use the MUSTANG instrument was desired during the course of this thesis work. A spare Hamamatsu Image Sensor and Driver/Amplifier board were available, so they were mounted in an aluminum box as shown in Figure 5-32. This provided the exact same pin connections that exist on the MUSTANG instrument. A window was cut out of the box to accommodated the photosensitive area of the image sensor. Various masks could be placed across this window to produce a geometric pattern in the spectrum obtained when reading out the photodiode array. This would allow for testing the MUSTANG interface circuit without having to use the MUSTANG instrument and delicate wavelength calibration lamps.

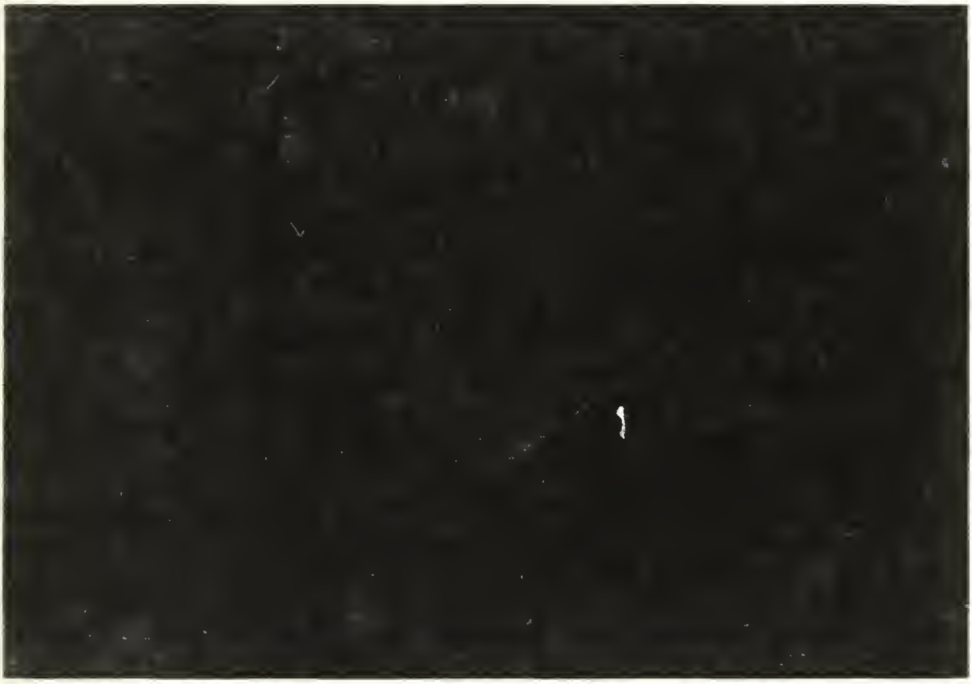


Figure 5-32 Spare Image Sensor Detector used in Interface Circuit Testing

VI. FLIGHT QUALIFIED INTERFACE CONSTRUCTION

The next chapter explains how the circuit design described in Chapter IV was validated. Once the design was validated, it had to be laid out to facilitate the manufacture of a printed circuit board (PCB). A PCB was necessary for the final flight-qualified interface circuit. All of the measurements and oscilloscope photographs shown in the next chapter were performed on the actual printed circuit boards.

A. PRINTED CIRCUIT BOARD DESIGN CONSIDERATIONS

Several factors came in to consideration when laying out the circuit design on a PCB. The first factor was the size constraint of the interface flight box enclosure. The interface box is fixed to the side of the HIRAAS instrument with four studs that are permanently attached to the titanium plate of HIRAAS. These studs are centered at the corners of a square that is three and one half inches on a side. The studs are long enough to accommodate a box that is two and one half inches high. There is physically enough room for a box that is approximately four and one half by four and one quarter inches with holes drilled for the mounting studs. Since the HIRAAS instrument is made of titanium, it was easier to construct the MUSTANG interface to fit the existing studs than to move the studs to accommodate a new design. These dimensions put a limit on the size of the PCB that could be used.

Due to circuit complexity and small area, a four-sided PCB was considered with a Power and Ground plane sandwiched between two signal trace layers. The additional features described in Chapter IV that were added to the revised interface circuit made it physically impossible to fit all of the necessary components on a single PCB. The design was spread out among two PCBs which could fit, parallel to eachother, within the height constraints of the interface box.

The next factor to consider in the design was how to divide the components up among the two PCBs. All of the components associated with the data collection were placed on one board. These included the A/D converter, FIFO memory buffer and the latches. All of the components associated with generating the proper command signals and the high voltage circuitry were placed on the other board. The command signals had to be passed to the other board via some external wires. This is not the most desirable method of interconnecting components, but could not be avoided in this case.

The final design consideration involved how to distribute power and ground to all of the necessary components. Appendix D and Appendix E recommend use of a low impedance ground for external connection of the analog and digital grounds of the A/D and D/A converters, respectively. The TTL outputs of the integrated circuits in the interface consist of a pair of transistors in a push-pull arrangement which generate large current transients during state transition. Due to the high number of digital signals running around on the PCB, noise spikes are likely to occur on the power and ground lines. The best way to remedy this situation is to use a large ground plane on one side of the PCB with bypass capacitors placed on the voltage supply of every integrated circuit. This results in much smaller spikes which travel smaller distances on the board [Ref. 11:pp. 599-600].

B. PRINTED CIRCUIT BOARD LAYOUT

The layout for the two PCBs was performed with a CAD tool on a personal computer. The *Tango PCB Plus* software package was used on an IBM computer. The layout was done by hand on the computer instead of using the auto-routing feature. The relatively small scope of this design made a hand layout feasible. This allowed for custom component placement which would give the shortest signal traces on the board. The boards were designed with a ground plane on the top layer, or component side of the board and the signal traces on the bottom layer. A silk screen was added to the top layer to show component placement, and a solder mask was added to the bottom layer. The layout files for each board layer were converted to a Gerber file format which was readable by the PCB manufacturer. The overall PCB composition is shown in Figure 6-1. Photoplot images of the PCB layers are shown in Figures 6-2 through 6-7.

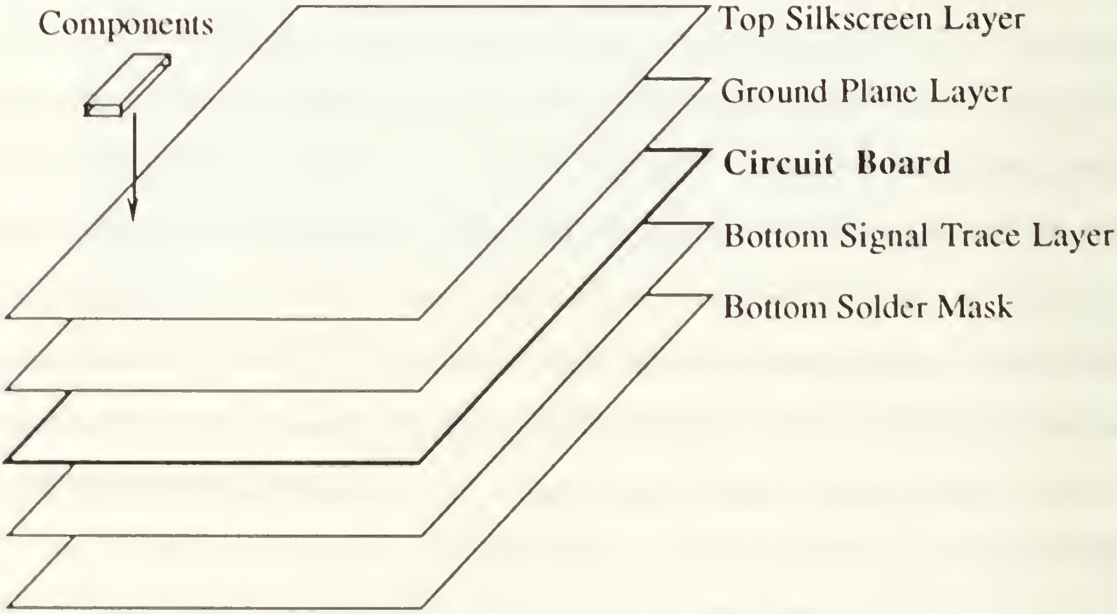


Figure 6-1 Printed Circuit Board Composition

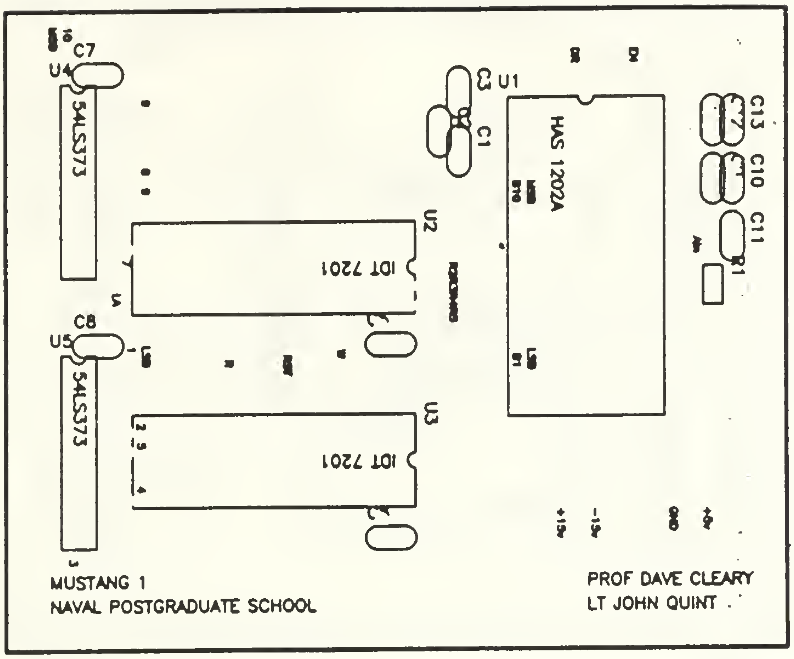


Figure 6-2 MUSTANG 1 Top Silkscreen Layer

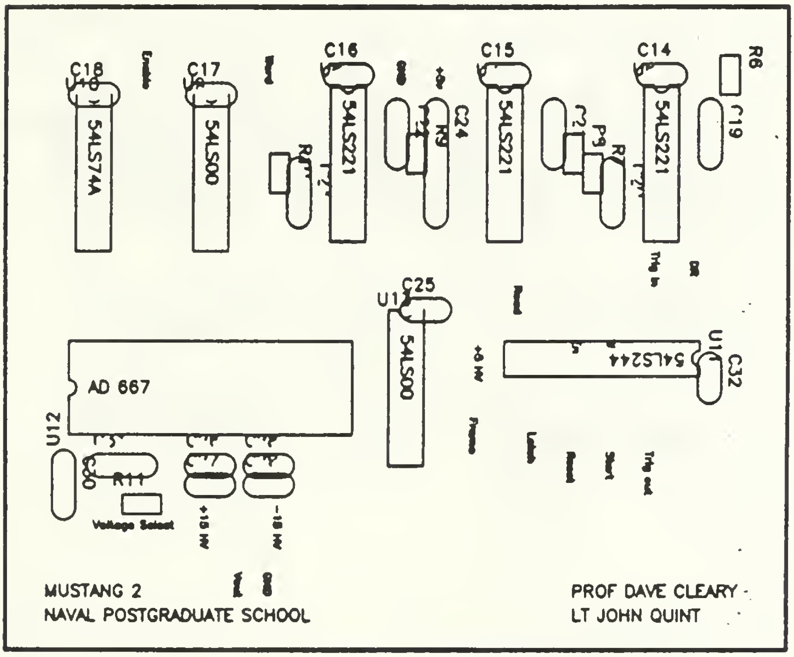


Figure 6-3 MUSTANG 2 Top Silkscreen Layer

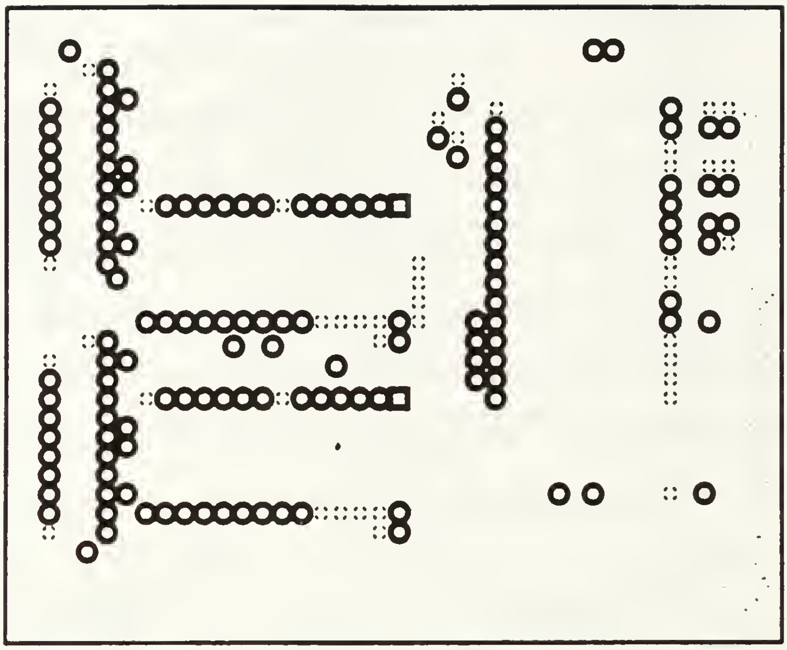


Figure 6-4 MUSTANG 1 Top Ground Plane Negative

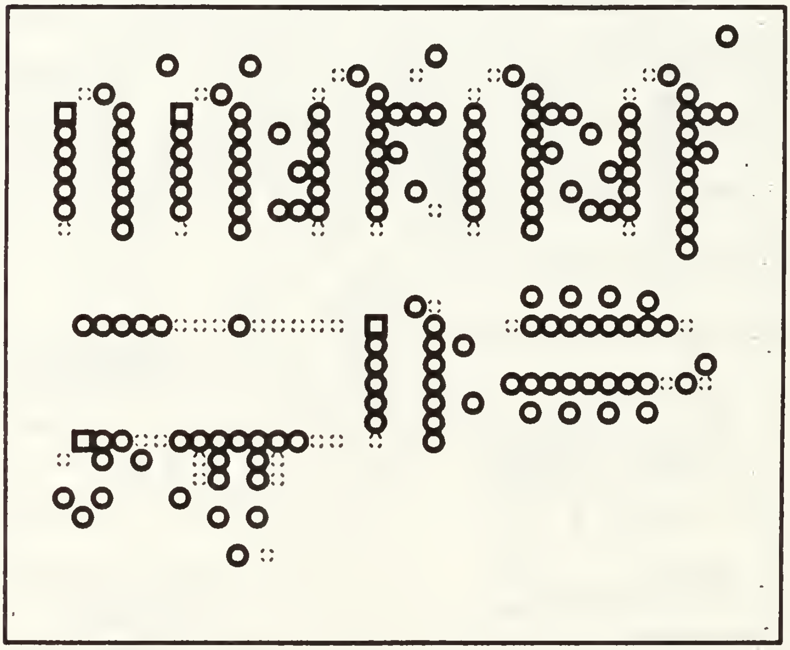


Figure 6-5 MUSTANG 2 Top Ground Plane Negative

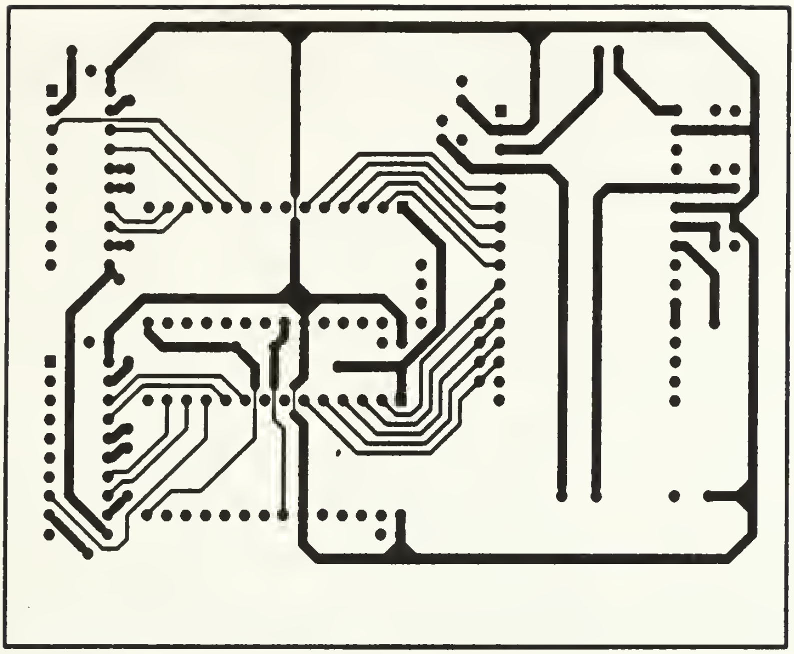


Figure 6-6 MUSTANG 1 Bottom Signal Traces

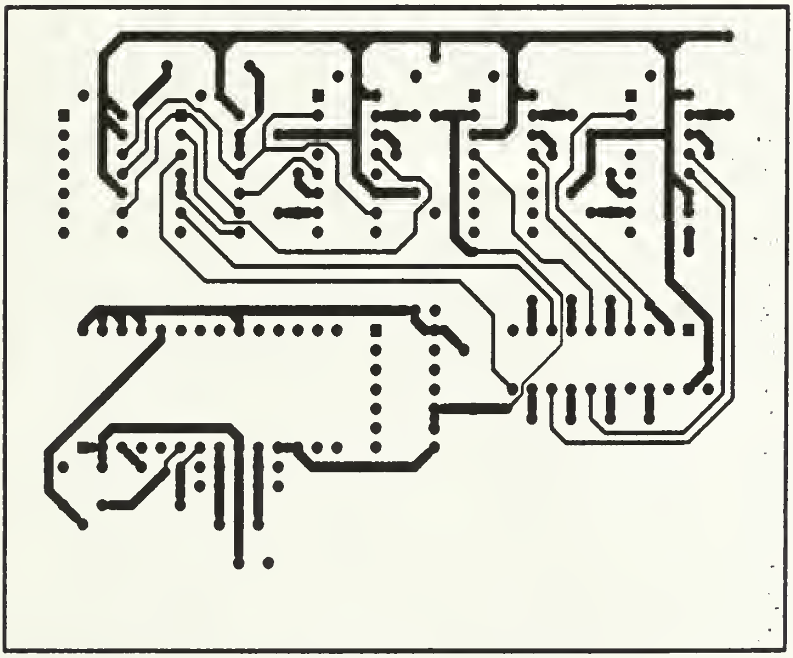


Figure 6-7 MUSTANG 2 Bottom Signal Traces

C. INTERFACE FLIGHT BOX ENCLOSURE DESIGN

A flight box enclosure was milled from a solid piece of aluminum in two halves. Each half of the enclosure houses one circuit board, and the two halves are bolted together for mounting with the MUSTANG instrument. The two halves of the enclosure are shown in Figure 6-8 and Figure 6-9 prior to conformal coating of the circuit boards. The PCB mounting screws provide a low impedance path from the ground plane on the boards to the enclosure casing. 25-pin D-sub connectors interface each circuit board to the MUSTANG wiring harness. Command signals which must travel between circuit boards are jumpered across the D-sub connectors. Figure 6-10 shows the flight-qualified configuration of the flight box enclosure and wiring harness mounted on the MUSTANG instrument. Pin assignments for the wiring harness are shown in Figures 6-11 and 6-12.

Figure 6-8 MUSTANG 1 PCB Flight Configuration

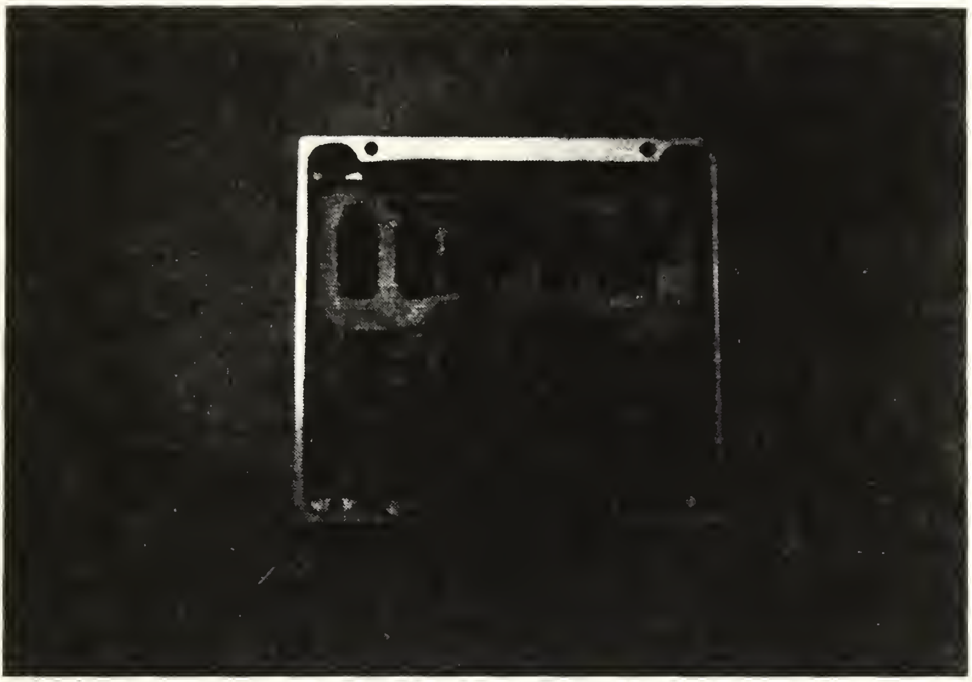


Figure 6-9 MUSTANG 2 PCB Flight Configuration

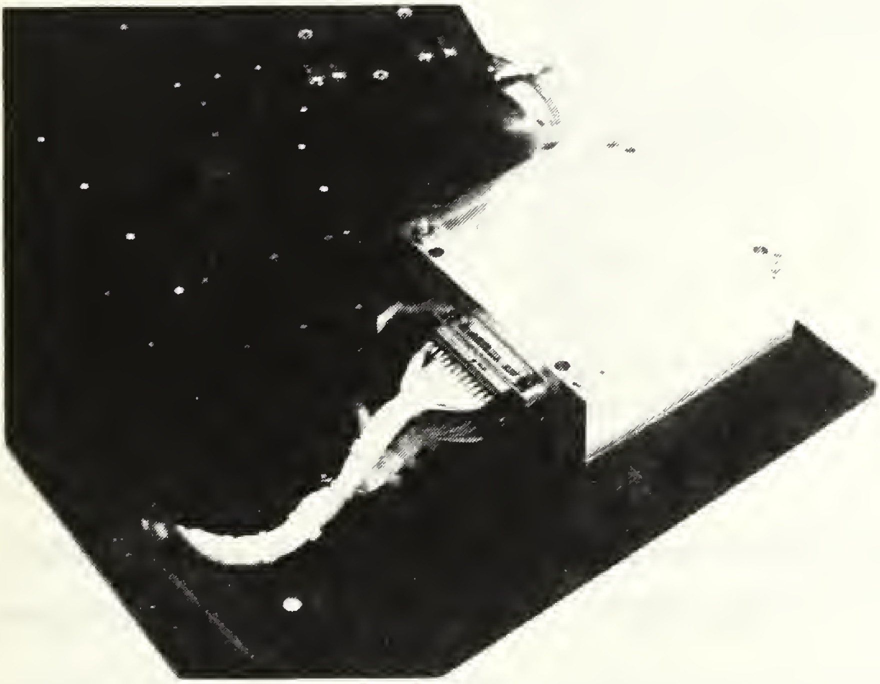
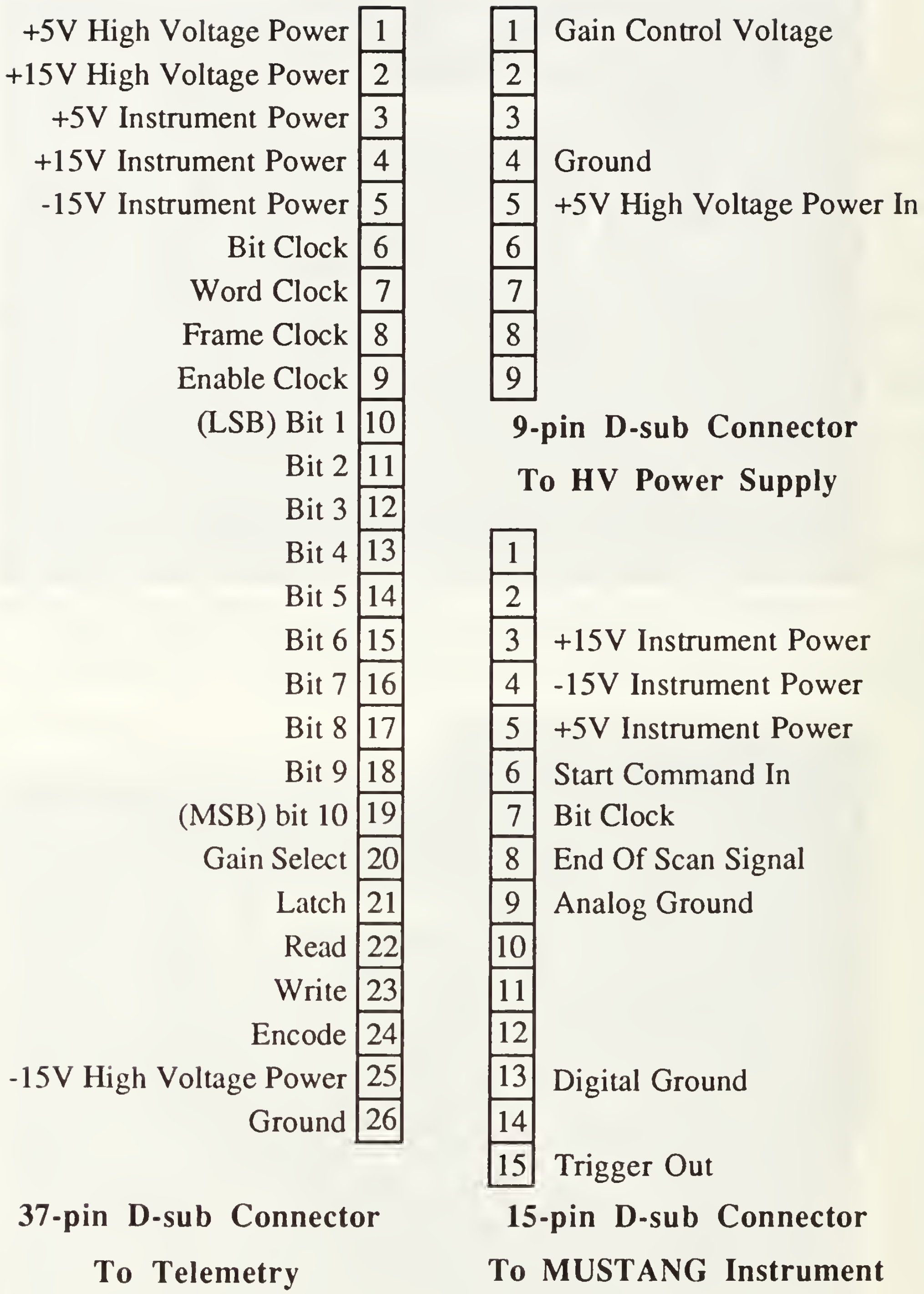


Figure 6-10 MUSTANG Interface flight Box and Wiring Harness



9-pin D-sub Connector
To HV Power Supply

37-pin D-sub Connector
To Telemetry

15-pin D-sub Connector
To MUSTANG Instrument

Figure 6-11 MUSTANG Wiring Harness Connections to Telemetry

Video Data Signal In (coax)	1	1	Data Ready In
	2	2	Trigger In
	3	3	Write Out
-15V Instrument Power In	4	4	Encode Out
+15V Instrument Power In	5	5	Read Out
Data Ready Out	6	6	Word Clock In
Reset Command In	7	7	Gain Select In
Latch In	8	8	
Bit 9	9	9	+5V Instrument Power In
Bit 6	10	10	+5V High Voltage Power In
(LSB) Bit 1	11	11	+15V High Voltage Power In
Bit 5	12	12	Ground (for control voltage)
Bit 3	13	13	Control Voltage Out
	14	14	Trigger Out
	15	15	Start Command Out
Ground	16	16	Reset Command Out
+5V Instrument Power In	17	17	Latch Out
Encode In	18	18	Frame Clock In
Write In	19	19	Enable Clock In
Read In	20	20	
(MSB) Bit 10	21	21	Ground
Bit 8	22	22	
Bit 7	23	23	-15V High Voltage Power In
Bit 2	24	24	
Bit 4	25	25	

25-pin D-sub Connector
MUSTANG 1 (top)

25-pin D-sub Connector
MUSTANG 2 (bottom)

Figure 6-12 MUSTANG Wiring Harness Connections at Interface Box

VII. INTERFACE CIRCUIT DEVELOPMENT AND TESTING

Testing of the MUSTANG electronic interface circuit occurred in several distinct phases. The design of the electronic interface was described in great detail in Chapter IV. The design, itself, was the subject of the first test. Although the design stands up to rigorous timing analysis on paper, it had to be validated with real integrated circuits and wires. This initial validation was done with a breadboard layout. When this functioned satisfactorily, a wire-wrapped prototype board was constructed. Since the design flaws of the original MUSTANG interface circuit were not discovered during laboratory testing, a foolproof method of testing the revised circuit had to be devised. The only way to be sure that the interface would function correctly in flight was to test it with the other flight components. A special trip was scheduled to NASA Goddard Space Flight Center, Wallops Flight Facility in Wallops Island, Virginia to test the interface with the Aydin Vector MMP-600 PCM Encoder providing the clocking signals. Once the circuit operation was demonstrated under flight conditions, the final flight-qualified circuit was constructed and subjected to rigorous tests at the formal rocket and payload integration at Wallops Island.

A. ORIGINAL BREADBOARD DESIGN VALIDATION

A breadboard was selected as the first medium on which to layout the redesigned interface circuit for several reasons. The breadboard is easy to work with, and provides its own power and some control signals for intermediate testing. Signal paths are easily traced on a breadboard circuit which aids in troubleshooting. Several alternatives can be quickly and easily compared by plugging and unplugging wires and integrated circuits. The breadboard does have several disadvantages, however. The circuit layout is inherently messy since wires must pass over the top of the circuit. The layout is generally very noisy with long wires adding significantly to stray capacitance. There is a large amount of coupling between signals which are physically adjacent on the breadboard.

The advantages above make the breadboard ideal for testing new designs. The first step was to get familiar with the operation of the different integrated circuits. Various control signals and outputs were studied for the A/D converter, D/A converter, FIFO, monostable multivibrator and other integrated circuits. Once all of the circuit components were fully understood, the circuit described in Chapter IV was constructed. Some important design considerations were addressed at this point. The data word to be stored in the FIFO memory was ten bits wide. The two FIFO integrated circuits could each store nine bits each, and the two latches could store eight bits each. The bits of the data word had to be divided between these components. Each component was MILSTD 883 Class B screened for high reliability, and no one integrated circuit was more prone to failure than any other. It was decided to split the bits evenly between the FIFO's and latches. Relative component placement in the layout was also considered to ensure short signal pathlength for minimum noise. The bit numbering scheme for the A/D converter was opposite to the convention used by the rocket payload wiring diagrams. Care had to be taken to ensure the most significant bit, (MSB), and least significant bit, (LSB), were kept in their proper orientation when delivered to the PCM encoder circuitry. A summary of the bit numbering notation is as follows.

- MSB = HAS 1202A Bit 1 (pin 5) = Rocket Payload Connector Bit 9 (pin 19)
- LSB = HAS 1202A Bit 10 (pin 14) = Rocket Payload Connector Bit 0 (pin 10)

The breadboard circuit was connected to the GSE described in Chapter 5 and found to operate correctly. The spare detector box was used as the source of analog signal input. A mask with three pinholes of various sizes was placed over the detector window, and a spectrum was obtained with the Macintosh II computer. The spectrum obtained had three features corresponding to light from the pinholes reaching the image sensor. The spectral features corresponded to the size and location of the pinholes in mask. This verified correct operation of the interface circuit design. The breadboard circuit is shown in Figure 7-1. The next step was to develop a wire-wrapped prototype circuit suitable for testing outside of the laboratory.

B. WIRE WRAPPED PROTOTYPE CONSTRUCTION

Wire-wrapped circuits on a good-quality vector board provide a much more durable and reliable circuit. High-reliability integrated circuit sockets were used for good connections at all components. Since the MUSTANG interface design had already been verified, the emphasis in this circuit construction was on circuit layout and neatness. An attempt was made to place components as they would be placed on the final flight-qualified printed circuit board. This gave an indication of the noise behavior of the final circuit with the components operating in close proximity to one another. D-sub connectors were mounted to the vector board, and the circuit was tested with the same laboratory GSE. The wire-wrapped prototype circuit is shown in Figure 7-2.

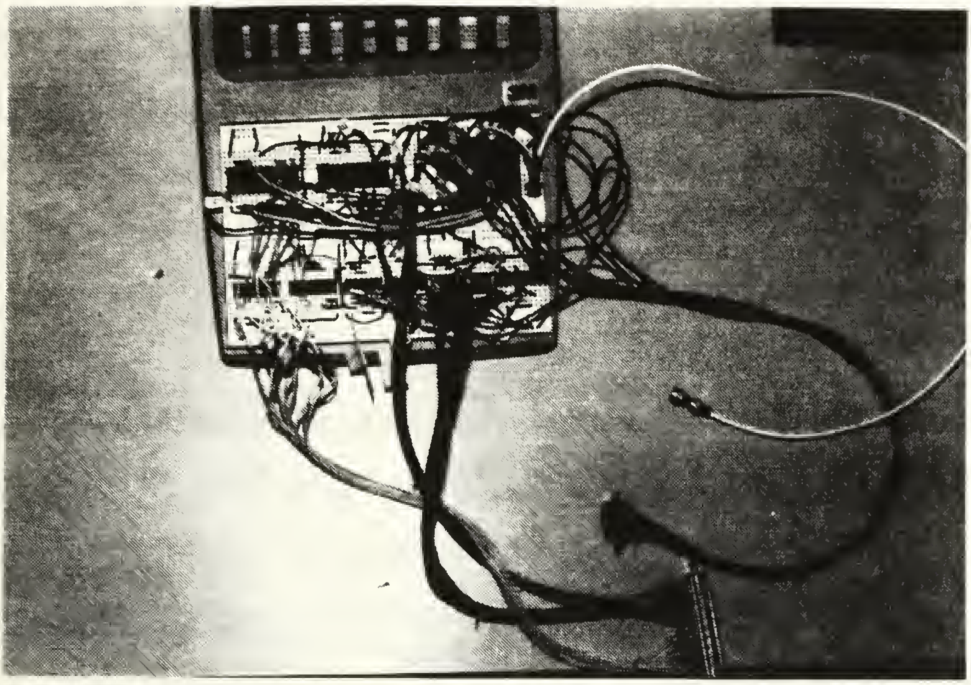


Figure 7-1 Breadboard Prototype Interface Circuit

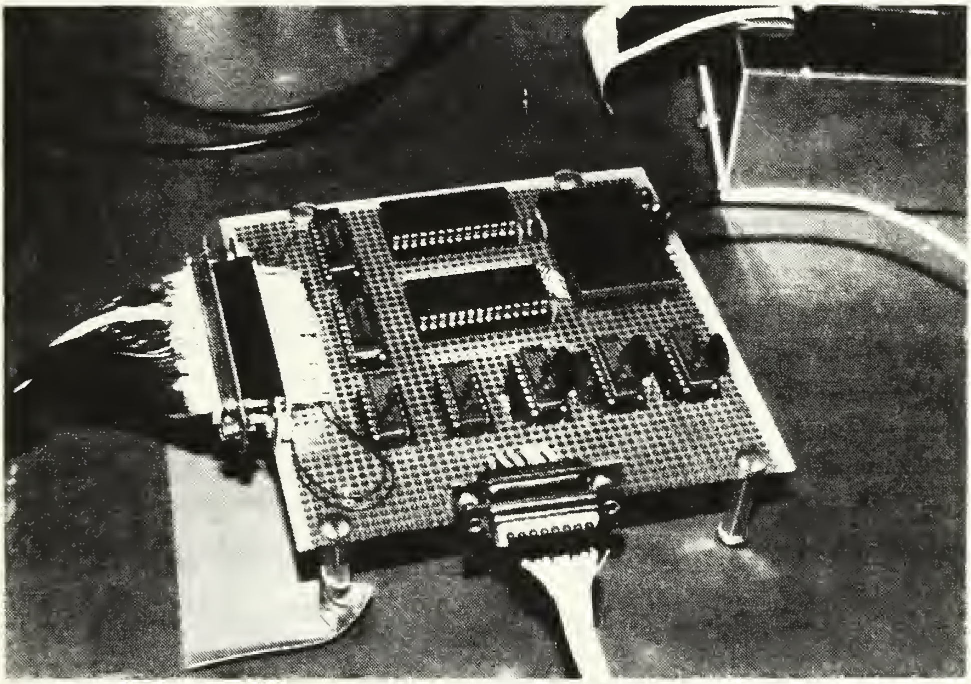


Figure 7-2 Wire-wrapped Prototype Interface Circuit

The main purpose of constructing the more rugged wire-wrapped circuit, was to allow for transportation to Wallops Island, and testing at the NASA, Wallops Flight Facility. A breadboard design would never have survived shipping intact. The breadboard circuit worked as expected in the laboratory GSE setup. The most important question to be answered was if it would work on the rocket with the PCM encoder supplying the synchronized clocking signals. A test was scheduled at Wallops Island, but a foolproof method had to be devised to ensure that all 512 photodiodes, actually made it to the rocket telemetry section.

Two methods were possible to test the circuit. The first method would be to hook it up to the MUSTANG instrument, and use one of the wavelength calibration lamps. The spectral components gathered by the MUSTANG would then have to be compared to the known spectral characteristics of the lamp. If a data shift occurred, as in the first MUSTANG flight, then we would know that data was being lost again. This method did not allow for ensuring that every single data word was getting through. It would only give a rough idea if the circuit was working correctly or not.

The second method involved using the spare detector. This eliminated the need for any type of calibration lamp or the MUSTANG instrument itself. The test would involve using some type of geometrical pattern on the spare detector. This alternative relied only on geometry to determine if every data word was getting through, and looked much more promising than evaluating an ultraviolet spectrum taken by the instrument. This method was selected as the best way to test the circuit. Several geometric patterns were evaluated for their ability to distinguish a single photodiode in the output data.

The pinhole mask produced a spectral feature that was much too broad to distinguish a single pixel. Next, a very narrow slit was constructed in front of the detector window with two razor blades. The blades were moved slightly apart at one end to produce a spectrum that looked like a ramp. The ramp spectrum had enough fluctuations in it to prevent its use in determining if a single word was lost in the spectrum. Next, the razor blades were used to make a uniform slit with a very thin wire placed perpendicular to the slit. The shadow cast by the wire on the image sensor was still approximately five pixels wide. This was too wide to determine each individual pixel. Finally, a satisfactory test was devised using a single razor blade and a micrometer rig. This test is described fully in the next section.

C. PRELIMINARY TESTING AT WALLOPS ISLAND

The prototype interface circuit and all of the GSE were transported to NASA Goddard Space Flight Center, Wallops Flight Facility in Wallops Island, Virginia. NASA provided the actual sounding rocket telemetry section for our use in the tests. The PCM encoder was programmed just as it was for the MUSTANG sounding rocket flight. The test micrometer rig and the spare detector were setup as shown in Figure 7-3 and Figure 7-4. The prototype interface circuit was connected to the PCM encoder, and to the spare detector. A light source was set up approximately 20 feet across the room to illuminate the detector. The overhead lights were turned off for the duration of the test described below.

A razor blade was attached to the micrometer with its edge vertical. The spare detector was positioned behind the razor blade relative to the light source.

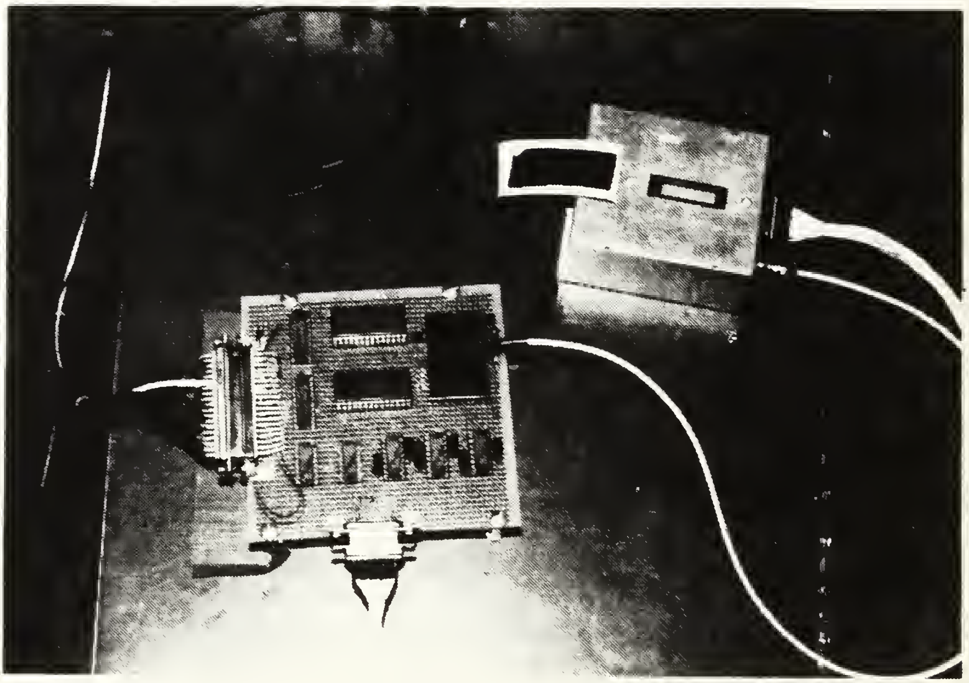


Figure 7-3 Electronic Interface Prototype Circuit and Spare Detector

Figure 7-4 Micrometer Rig and Spare Detector Test Setup

The micrometer travel was horizontal so that as the razor blade moved, it obscured from the light source each successive photodiode on the image sensor.

1. Testing of the Original Electronic Interface Circuit

The first test conducted with the micrometer test rig was of the original MUSTANG interface circuit. In order to validate past analysis on the MUSTANG flight data, it was desired to verify that every 17th data word was really dropped out. It was also desirable to determine if any extra data words were really dropped out, and if so, the location in the spectrum of the lost words. The 512 data words from the original MUSTANG interface were observed on the ground station computer. The micrometer was translated in 50μm increments, since that is the pitch of an individual photodiode on the linear image sensor as described in Chapter II. The photodiodes in the linear array that were exposed to the light, produced a uniform value at the output observed in the telemetry computer. The photodiodes in the shadow of the razor blade produced a significantly lower value at the output. It was possible to determine from the output observed on the telemetry computer, the location of the razor blade edge to within a single pixel location. This made it possible to uniquely identify every single pixel in the spectrum produced by the image sensor. As the micrometer was rotated another 50μm, one pixel in the output would go from a high to a low value indicating that it was being shaded by the razor blade. A slight amount of diffraction was exhibited by the light passing the edge of the razor blade, but each individual pixel could easily be identified in the output.

When the micrometer was translated, and the computer output did not change, there was indication that the data from the photodiode at that location was being lost. The test verified that every 17th data word in the spectrum was, in fact, lost as suspected. Three additional data words were found to be lost from the spectrum at pixel locations 103, 240 and 376. This data loss was exactly as predicted in the data analysis performed on the MUSTANG flight data [Ref. 3:p. 72]. The results of this test are summarized in Appendix L. The location of all lost data words in the spectrum is identified in this Appendix, along with the corresponding wavelength for each pixel. This data assumes 3.133Å wavelength per pixel.

2. Testing of the Revised Electronic Interface Prototype Circuit

The revised electronic interface circuit was tested under the exact same conditions as the original circuit described above. The micrometer rig was moved over the entire length of the image sensor. Every single photodiode was found to be represented in the output spectrum indicating that no data words were lost. This test positively verified the functionality of the revised interface circuit. The next phase of development was to produce the printed circuit boards described in Chapter VI for construction of the final flight-qualified interface circuit.

D. VALIDATION OF FLIGHT-QUALIFIED CIRCUIT

Several copies of the two printed circuit boards were manufactured by West Coast Circuits, Inc., in Watsonville, California. High-reliability integrated circuit sockets were used with the first set of printed circuit boards. The circuit boards were secured in the flight interface box and attached to the MUSTANG instrument. The circuit was verified to operate properly when tested from the laboratory GSE setup. The clock synchronization waveforms produced by the GSE were discussed in Chapter V All other control waveforms generated by the interface circuit are presented in this section for verification of proper operation.

1. Driver/Amplifier Board Signals

The Hamamatsu Driver/Amplifier circuit within the MUSTANG instrument needs only two control signals for its operation, a system clock and a start command. The system clock is the same as the Bit Clock produced by the GSE as shown in Figure 5-2. The Start command is produced by the interface circuit and is shown, along with the Frame Clock, in Figure 7-5. The Start command is produced by a monostable multivibrator as described in Chapter IV. It was configured to be a positive pulse of approximately 6.53µs duration triggered by the rising edge of the Frame Clock pulse. The Frame Clock as described in Chapter V, is high for one data word in 1024. The duration of the Frame Pulse is 50µs and the period is 51.2ms. The Start pulse in Figure 7-5 rises with the rising edge of the Frame Clock pulse and falls approximately 6.5µs later, as designed. The Reset command, shown in Figure 4-1, is used to reset the FIFO memory at the beginning of each frame of data. It is derived from the complementary output of the same monostable that generates the Start pulse. The Reset pulse is just the inverted signal of the Start pulse and is not shown here.

The Hamamatsu driver/amplifier circuit provides the Trigger signal which pulses high each time the analog signal read out from a new photodiode is stable. The Trigger pulse duration is 5µs and a new pulse occurs every 20µs. The Trigger signal is shown in relation to the Bit Clock in Figure 7-6.

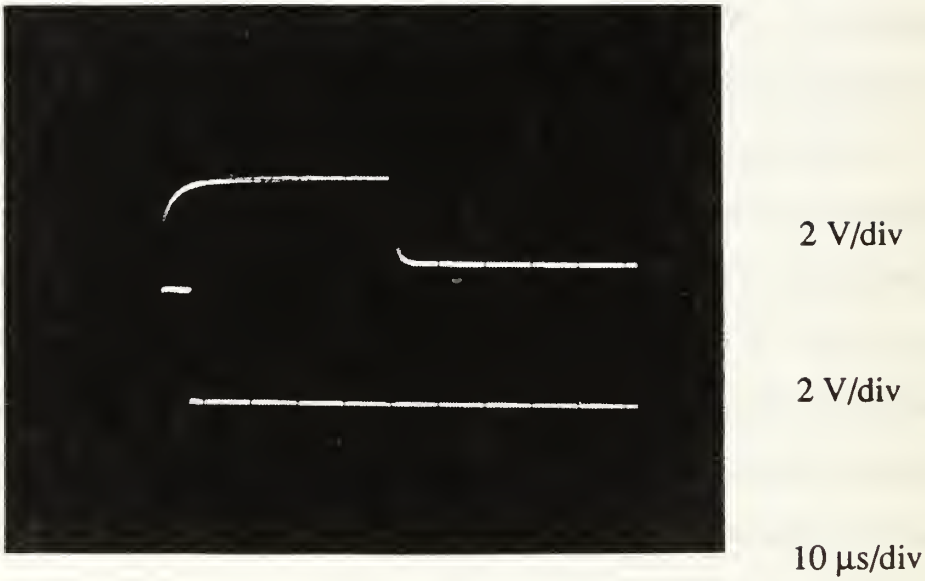


Figure 7-5 Frame Clock (top) and Start Command Signal (bottom)

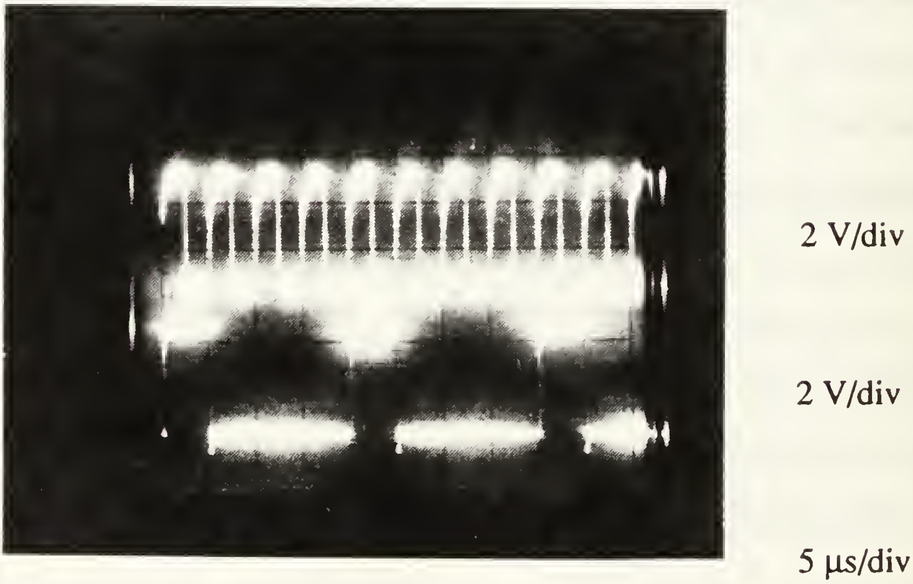


Figure 7-6 Bit Clock (top) and Trigger Signal (bottom)

2. Data Acquisition From the MUSTANG Instrument

The data from the MUSTANG instrument is in the form of an analog voltage. The analog signal is referred to as Video Data. This analog voltage is delivered to the interface circuit via a coaxial cable, and must be accepted when the Trigger control signal is high. The command signals discussed in Chapter IV for digitizing and storing the analog voltage are shown in this section.

a. Command Signals

An Encode command is generated with a monostable multivibrator on the rising edge of the Trigger signal. This command pulse tells the A/D converter that the analog input voltage is constant, and ready to be digitized. The positive Encode pulse was configured to have a duration of 525ns and is shown in Figure 7-7 along with the Trigger signal that initiates it.

The Data Ready signal is a positive pulse generated by the A/D converter. The Data Ready pulse goes high after the Encode pulse goes high to signify that the data conversion process has started. Data Ready goes low when the data conversion process is complete signifying that the digital word representing the analog signal has been latched and is available at the output pins. Figure 7-8 shows the Data Ready signal compared to the Trigger signal. Figure 7-9 shows the Data Ready signal compared to the Encode command signal. The Data Ready signal is supposed to go high approximately 60ns after the rising edge of the Encode command, and this is verified in Figure 7-9. The data conversion in the A/D converter is supposed to take no longer than 1.46μs plus the duration of the encode command. Figure 7-9 shows that the data conversion is complete in approximately 1.80μs, which is well within the specification.

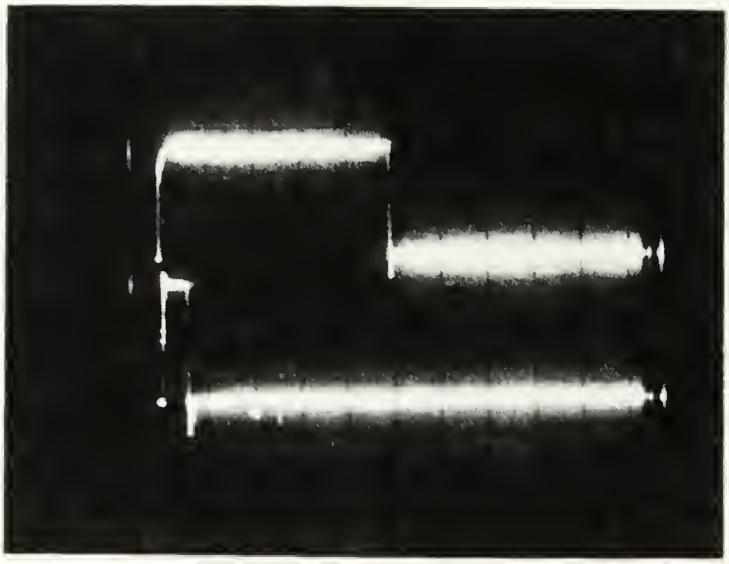


Figure 7-7 Trigger Signal (top) and Encode Command Signal (bottom)

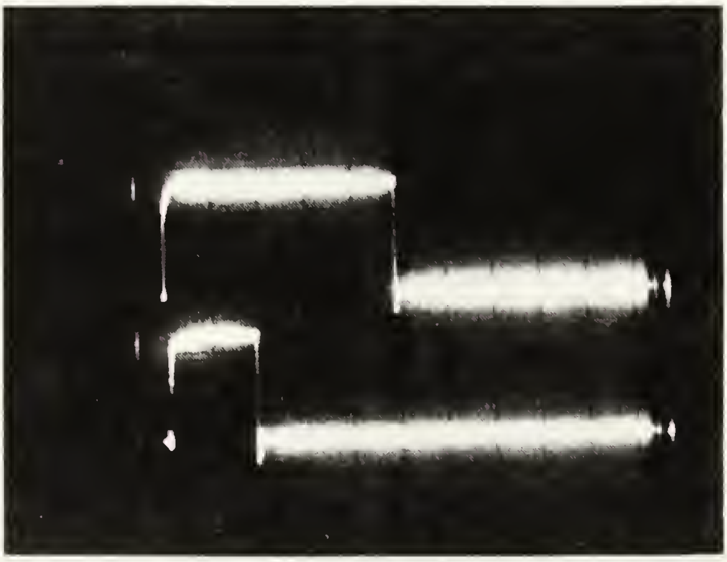


Figure 7-8 Trigger Signal (top) and Data Ready Signal (bottom)

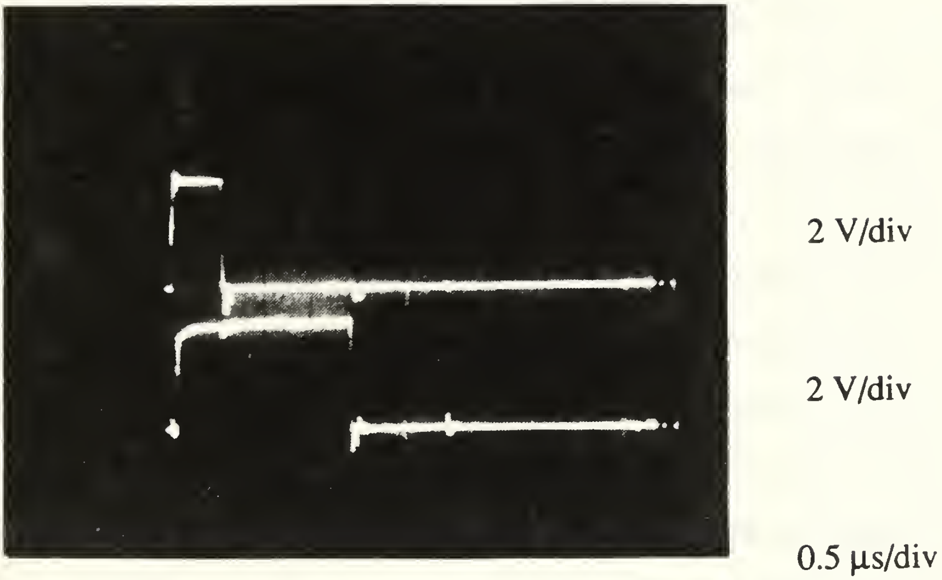


Figure 7-9 Encode Command Signal (top) and Data Ready Signal (bottom)

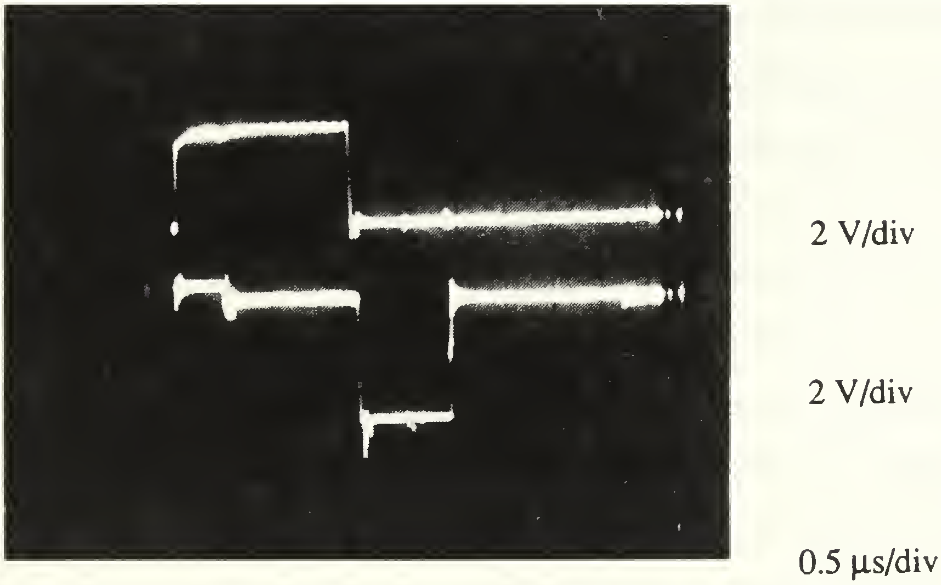


Figure 7-10 Data Ready Signal (top) and Write Command Signal (bottom)

The Write command signal tells the FIFO that the digital data out of the A/D converter is valid and should be latched into the FIFO. This negative pulse is also generated by a monostable triggered from the falling edge of the Data Ready signal. The Write command signal is shown in relation to the Data Ready signal in Figure 7-10. The Write pulse duration was configured to be 0.98µs, and it is verified to be just less than one microsecond in Figure 7-10. Close inspection of this figure reveals that there is a noticeable propagation delay for the monostable in generating the Write command pulse. The falling edge of the Write signal occurs several tens of nanoseconds after the falling edge of the Data Ready signal as predicted in Figure 4-2.

Another feature apparent in the Write command signal of Figure 7-10 is the significant noise present in the first 0.5µs of the oscilloscope trace. This noise is due to the Encode command which goes low at that time. This can be verified from Figure 7-9. This noise, while significant, does not cause any problems in the control of the interface circuit. The noise is in no danger of being interpreted as a false Write command signal. This digital noise did, however, find its way into the analog voltage signal from the MUSTANG instrument which had to be corrected in the final design.

b. Digital Noise Imposed on the Analog Voltage Signal

In the original MUSTANG interface circuit, the digital and analog grounds were all connected together via a ground plane which filled one side of the printed circuit board. This meant that any digital noise caused by transitions in all of the command signals, could reach the analog voltage signal through the ground plane. In an effort to prevent this noise in the analog signal, the coaxial shield around the analog signal line was not connected from the driver/amplifier circuit to the SMA connector on the MUSTANG instrument. This intended fix, in fact, had the opposite effect. The analog voltage signal produced by the image sensor on the driver/amplifier circuit is referenced to an analog ground on the driver/amplifier board. The analog ground is tied to the digital ground on the driver/amplifier circuit, and this cannot be altered. The analog voltage signal traveled down a coaxial cable to the interface circuit to be digitized by an A/D converter. The ground, that this analog signal was referenced to, was not passed to the interface circuit, but was interrupted by the open circuit at the SMA connector on the MUSTANG instrument.

Effective signal grounding and shielding is a complex science to the extent that it could almost be called an art. The ideal system ground would be a single point. Since circuits and components have physical size, a point ground is not feasible. Instead, the ground must be distributed around to all components on a plane, through wires or through metal casings of circuit enclosures and instruments. This leads to multiple paths or loops in the ground paths between components in the system. The ground elements are therefore exposed to magnetically induced currents and other phenomena which result in potential differences throughout the ground system.

In the case of the original MUSTANG configuration, the ground that the analog signal was referenced to was not at the same potential as the ground on the interface circuit. The coaxial cable in the spare detector box is not grounded to the box itself. This is the same as the configuration in the MUSTANG instrument. Figure 7-11 was obtained using the Video Data signal out of the spare detector circuit and the revised interface circuit. The Video Data signal of approximately two volts is shown in reference to the Trigger signal. The Trigger signal initiates all of the data conversion process, indicating that the analog voltage is stable. There is clearly a lot of noise in the analog signal while the Trigger signal is high. Voltage swings of the noise spikes are nearly one volt peak-to-peak, and are due to the digital transitions of the control signals as will be explained later. The spikes are so large simply because the ground potential at the driver/amplifier circuit is not the same as the ground potential at the A/D converter.

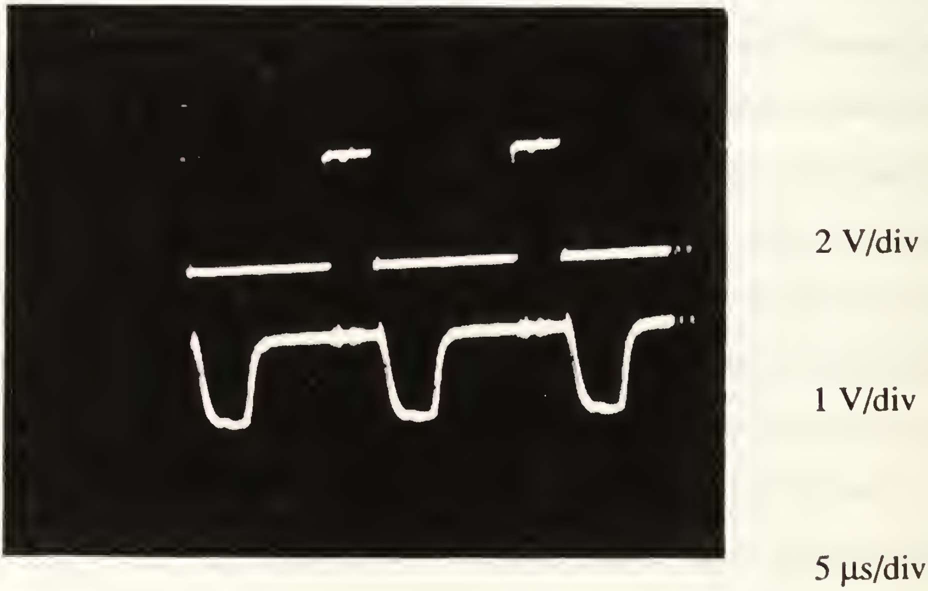


Figure 7-11 Trigger Signal (top) and Unreferenced Video Data Signal (bottom) before connecting coaxial shield

c. Modifications to Reduce Noise in the Analog Voltage Signal

The first correction to decrease the noise present on the analog signal was to reconnect the coaxial shield from the driver/amplifier circuit to the SMA connector on the MUSTANG instrument. This ensured a contiguous ground shield from the origin of the Video Data signal, all the way to the A/D converter. The results of this modification were rather spectacular, and are shown in Figures 7-12 and 7-13. These figures were obtained by viewing the Video Data signal from the MUSTANG instrument with only instrument power applied. The high voltage circuit was not energized, so the instrument output was due only to dark current. The Video Data signal amplitude is only about 80mV, and the noise has been reduced to approximately ±40mV. This is a very significant improvement.

The origin of the noise spikes can easily be determined from the figures. Figure 7-12 shows the Video Data signal in reference to the Encode command signal. The Encode command pulse transitions are responsible for the first two noise spikes on the Video Data signal. Figure 7-13 shows the Video Data signal referenced to the Data Ready signal. The falling edge of the Data Ready signal is responsible for the next noise spike visible in the Video Data signal. The fourth noise spike is due to the rising edge of the Write command pulse which is not shown in these figures. Close inspection also will show that there are smaller noise spikes that occur at 2.5μs intervals which correspond to transitions of the Bit Clock.

The ten most significant bits are being used on the A/D converter which is set for 8.24V full scale. This corresponds to approximately 8.05mV

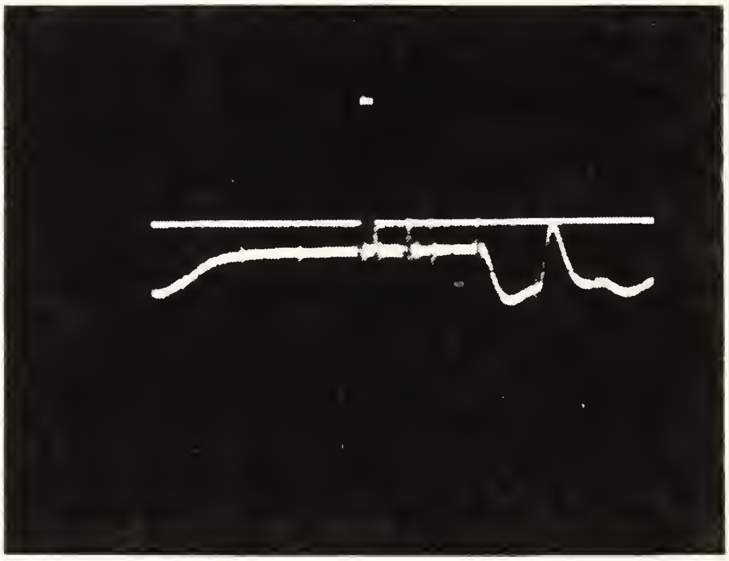


Figure 7-12 Encode Command Signal (top) and Video Data Signal (bottom) after connecting coaxial shield

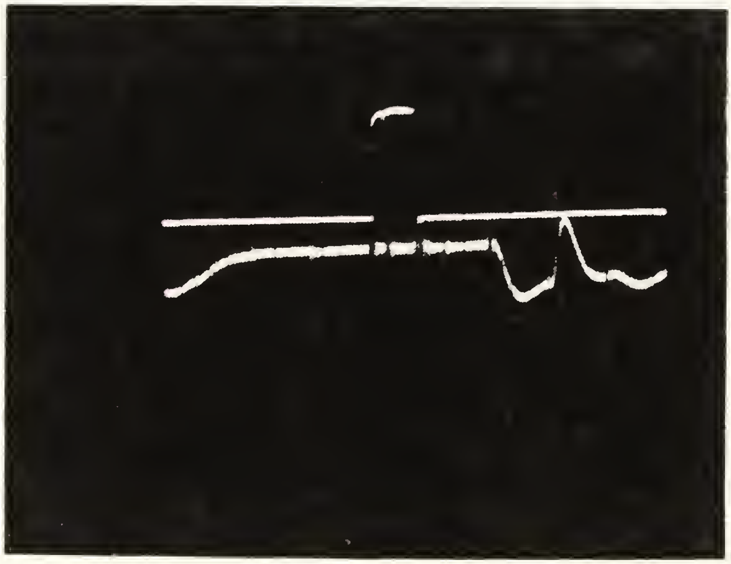


Figure 7-13 Data Ready Signal (top) and Video Data Signal (bottom) after connecting coaxial shield

resolution in the digitized signal. The noise observed in Figures 7-12 and 7-13 indicates that the low three or four bits would vary with noise. After the Encode command pulse goes low, the analog voltage signal is relatively noise free until A/D conversion is complete. This allows for a quiet environment in which the current-output D/A converter, successive approximation register and high speed comparator can digitize the analog signal within the A/D converter. Pulldown resistors were placed on the four least significant bits to aid in sinking current for transitions in a noisy environment as suggested in Appendix D. All of the noise that occurs in the analog signal after the digitizing is complete is not of concern. The digital data bits are latched in the successive approximation register with the falling edge of the Data Ready pulse.

One additional attempt to reduce the noise on the analog voltage signal was to separate the analog and digital ground at the interface circuit. It was hoped that isolating the analog ground of the A/D converter from the digital ground plane of the interface circuit would reduce the noise seen in Figures 7-12 and 7-13. A portion of the ground plane on the printed circuit board was carved out to accommodate the analog ground pins of the A/D converter and the same measurements were taken. Unfortunately, this resulted in slightly higher amplitude noise spikes. The recommendation of Appendix D, for a low impedance ground plane to connect the analog and digital ground pins of the A/D converter, was followed, and the ground plane was left intact on the flight-qualified interface circuit boards.

3. Data Transfer to the PCM Encoder

As mentioned in Chapter IV, this portion of the interface circuit was the most important as far as timing analysis was concerned. The gated Enable signal was created to be synchronous with the falling edge of the Word Clock. This is shown in Figures 7-14 and 7-15. These figures show the gated Enable signal in reference to the Word Clock. The gated Enable signal rises with the falling edge of a Word Clock pulse, and falls with the falling edge of the Word Clock for the 17th data word.

The Read command signal is shown in reference to the gated Enable signal in Figures 7-16 and 7-17. This is the most critical signal in the interface circuit since it was the source of data loss in the original MUSTANG interface circuit. The first Read command pulse is shown in Figure 7-16, and it goes low immediately with the rising edge of the gated Enable signal. This validates the design described in Chapter IV. All 16 Read command pulses were counted while the gated Enable signal was high on the expanded time scale mode of the oscilloscope. No glitch of any kind is apparent on the Read command line from Figure 7-17 after the gated Enable signal goes low. This verifies that no extra Read command pulses will be generated in the interface circuit; therefore, no data will be lost.

The negative Read command pulses were created from a monostable multivibrator, and configured to be 2.8μs in duration. The Read pulse was triggered on the rising edge of the inverted Word Clock which is shown by its relationship to the gated Enable signal in Figure 7-16. The duration of the Read command pulse is verified in Figure 7-18 where the Read pulse is shown as compared to the Latch command pulse. The positive Latch pulse is also generated from a monostable triggered from the same edge as the Read pulse. The Latch pulse duration was configured to be 2.1μs. Figure 7-18 shows that the

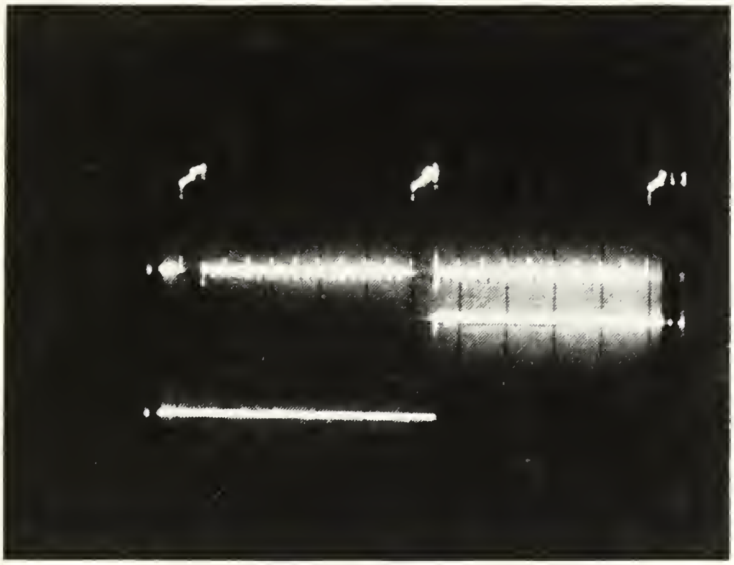


Figure 7-14 Word Clock (top) and Gated Enable Signal Rising Edge (bottom)

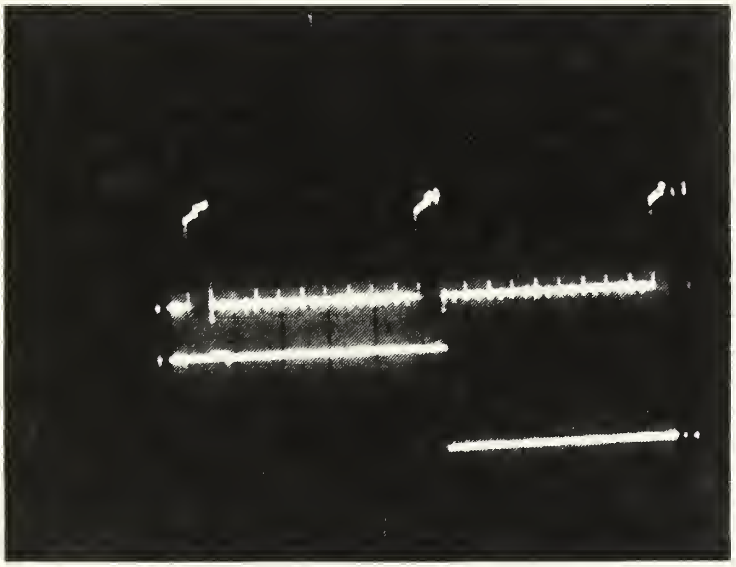


Figure 7-15 Word Clock (top) and Gated Enable Signal Falling Edge (bottom)

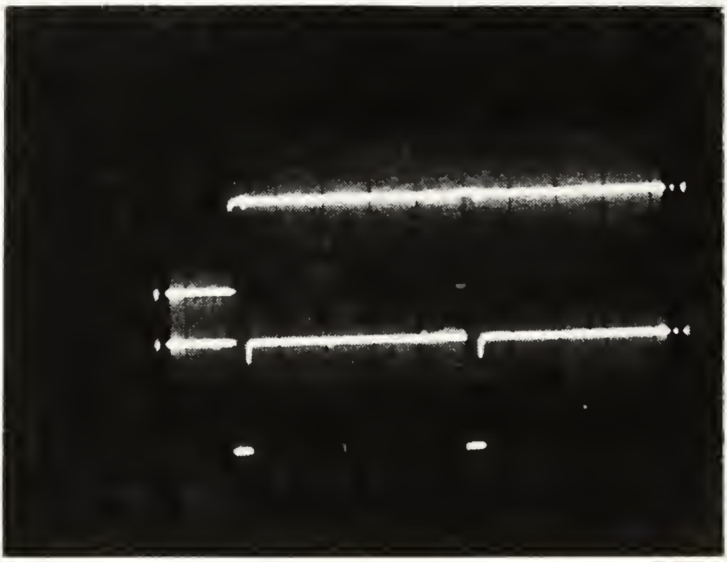


Figure 7-16 Gated Enable Signal Rising Edge (top) and Read Command Signal (bottom)

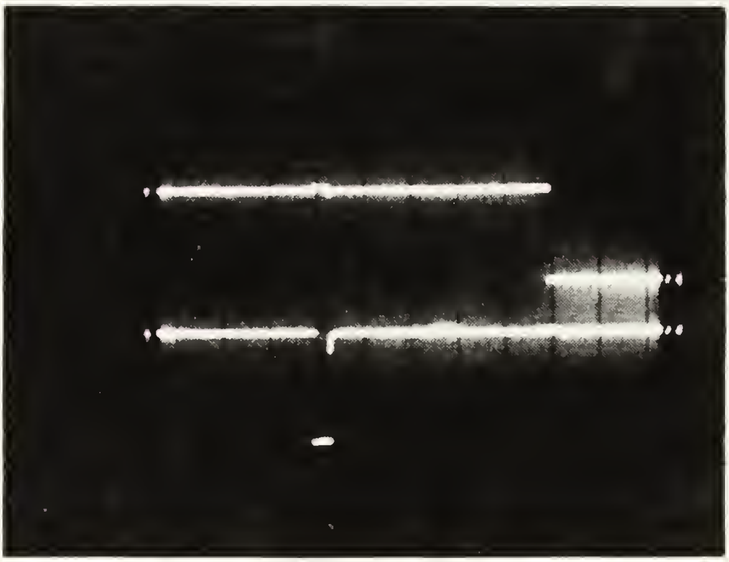


Figure 7-17 Gated Enable Signal Falling Edge (top) and Read Command Signal (bottom)

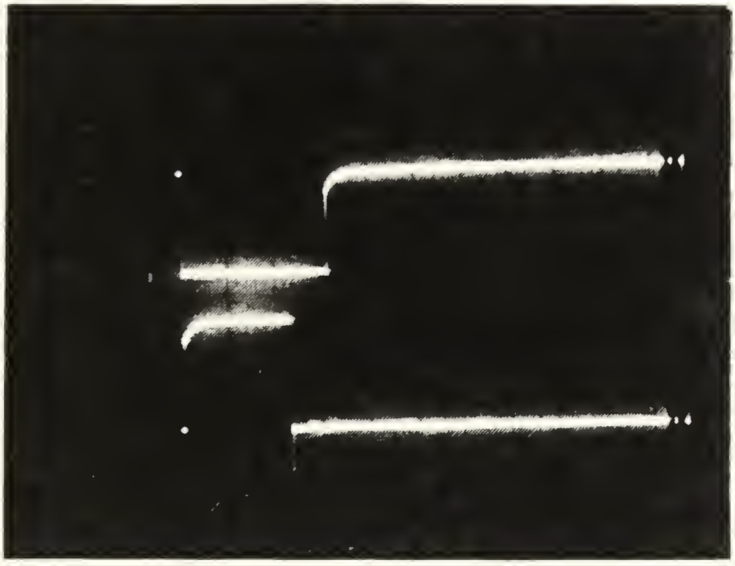


Figure 7-18 Read Command Signal (top) and Latch Signal (bottom)

Read pulse ended up about 3.2µs, and the Latch pulse about 2.3µs which fulfills the requirements of the circuit design in Chapter IV.

4. Instrument Gain Control Voltage

The instrument gain control voltage was measured with a multimeter at the output of the D/A converter. The measured voltages listed below are consistent with the calculated voltages from Figure 4-5.

- Measured High Gain Control Voltage = 9.706V
- Measured Low Gain Control Voltage = 9.394V

Due to the extreme sensitivity of the instrument gain to this control voltage, it was imperative that this analog voltage be noise free. The analog voltage was observed on an oscilloscope, and a significant amount of noise was present. This noise was believe to be a product of the test setup. A differential measurement was performed using the oscilloscope and two probes with their leads twisted together. No noise was observed beyond the accuracy of the measurement which was 20mV peak-to-peak.

E. ROCKET INTEGRATION TESTING AT WALLOPS ISLAND

The MUSTANG instrument was taken to the Naval Research Laboratory where it was integrated with the HIRAAS instrument. The MUSTANG physically attaches to the side of HIRAAS in the Experiment section of the rocket. It was tested in this configuration with the Launch GSE supplying telemetry clocks, and was found to function without problem.

The rocket Experiment section was transported to Wallops Flight Facility for the full rocket integration testing. All sections of the rocket were first connected electrically, and a series of sequence tests were performed. The sequence test performs an actual launch countdown, and all flight timers and relays are tested to ensure that the preprogrammed events happen according to the flight schedule. A brief summary of major flight events are as follows.

• -120 seconds	Begin countdown
• -30 seconds	Rocket on internal power
• 0 seconds	Terrier ignition
• 12 seconds	Black Brant ignition
• 44 seconds	Black Brant burnout
• 60 seconds	Rocket despin
• 63 seconds	Payload separation
• 66 seconds	Nose cone eject, Experiment section door opens
• 85 seconds	MUSTANG instrument power applied
• 96 seconds	MUSTANG high volts power applied
• 293 seconds	Switch to high gain
• 490 seconds	Switch to low gain

- 510 seconds MUSTANG high volts power off, close door
- 516 seconds MUSTANG instrument power off
- 605 seconds Deploy parachute

The MUSTANG performed with no problems during all of the sequence tests. All sections of the rocket were then bolted together in their final launch configuration for environmental testing. The environmental tests determine the mechanical characteristics and integrity of the rocket and payload. These tests consist of the following.

- Moment of inertia determination
- Weight determination
- Center of gravity determination
- Spin balance
- Three-axis random vibration tests
- Operational spin test

Following environmental testing, the rocket is subjected to another series of sequence tests to ensure that it still functions properly after all of the mechanical tests. The MUSTANG passed all of the integration tests and is ready for launch in February 1992.

VIII. CONCLUSIONS

The success of MUSTANG on the NASA sounding rocket experiment in March, 1990 has established NPS and the MUSTANG project in the scientific research community. The rocket flight produced the best measurements to date of ultraviolet emissions in the earth's ionosphere in the middle ultraviolet wavelength region. Despite the success of this flight, some problems with the electronic interface package were manifested in the telemetry data recovered from the flight. Continued NASA support for the joint NPS and NRL research is exhibited in the scheduling of a second sounding rocket experiment (36.088DE) for the MUSTANG and HIRAAS instruments which will launch in February, 1992.

A. SUMMARY OF MUSTANG DEVELOPMENT

This thesis involved redesign of the MUSTANG electronic interface package to prevent the data dropouts which occurred during the first sounding rocket flight. An in-depth analysis of the MUSTANG instrument and the sounding rocket components was necessary to determine the cause of the data dropouts and to formulate a new circuit design. The interface circuit redesign included the following major elements.

- Review of the operational limitations of the MUSTANG instrument and the PCD linear image sensor to determine necessary interface requirements.
- Review of the interface requirements for the NASA-provided PCM encoder which was believed to be the cause of the majority of the data dropouts.
- Study of the original MUSTANG interface electronic interface circuit to locate possible sources of faults which would lead to data dropouts

- Propose a new circuit design which would interface with existing rocket and experiment hardware to reliably transfer data to telemetry during rocket flight without the risk of data dropout.
- Construct a prototype of the revised interface circuit, and validate its proper performance through testing in the laboratory.
- Determine the cause of the data dropouts with the original interface circuit through testing at Wallops Flight Facility with an actual telemetry section from a sounding rocket. Additionally, verify proper performance of the revised interface circuit prototype with the same test setup.
- Design and fabricate the final flight-qualified components, and install them on MUSTANG
- Participate in the formal payload integration for NASA sounding rocket flight 36.088DE in October, 1991 at Wallops Flight Facility in Wallops Island, Virginia to ensure the proper operation of MUSTANG in the flight environment.
- Design and implement all changes in the MUSTANG GSE hardware and software necessary to support the revised interface circuit. Additionally, implement changes in the GSE to make it more user friendly for new students unfamiliar with the operation of MUSTANG.

Participation in the MUSTANG development and integration provided NPS students with an informative view of the scientific research community as well as the DoD program environment. The opportunity to work with NPS faculty, NRL scientists and NASA technicians and engineers in this research project provided insight not attainable in the classroom environment. The exposure to such areas as program management, production scheduling, parts procurement, compatibility design, component integration and electronic noise reduction provided by MUSTANG research is essential to the development of the engineering student.

B. PROSPECTS FOR FUTURE ENHANCEMENTS AND FOLLOW ON THESIS WORK

The MUSTANG electronic interface circuit constructed as a result of this thesis work performed flawlessly during payload integration for NASA rocket experiment 36.088DE. The MUSTANG instrument is expected to operate without incident on the upcoming launch in February, 1992. Data recovered from the upcoming launch are expected to be even better than the first launch, with no data dropouts to complicate analysis. The only component of the MUSTANG project that is below optimum performance is the launch GSE interface box. Future enhancements could concentrate on improving the performance of this piece of GSE hardware. The current design is adequate, but a concentrated effort would be necessary to bring this piece of GSE equipment up to desired performance. The MUSTANG instrument is tentatively scheduled to make one additional NASA sounding rocket flight following the upcoming scheduled launch. This additional launch would make the upgrade of the launch GSE a worthwhile topic of research for an interested Space Systems Engineering student with an Electrical Engineering background.

Additionally, the MUSTANG instrument is to be one of many instruments launched on the Air Force P91-1 satellite in the Fall of 1995. The MUSTANG will be delivered for integration on the satellite in the Fall of 1994. The opportunity for future work by NPS students on the MUSTANG project is guaranteed and wide in scope. The interested Space Systems Operations student could follow the program management and integration of an actual NPS instrument onto a low earth orbit satellite. The interested engineering student could get involved with the design of the flight microprocessor-controlled MUSTANG interface with the satellite bus. Substantially different data acquisition and storage methods, and time-shared data transfer will provide a great deal of future research work. As long as the MUSTANG continues to be successful, there will always be a need for research in the analysis of the data it provides to validate current photochemical models of the ionosphere, and to determine ionospheric electron densities.

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APPENDIX A

HAMAMATSU PCD IMAGE SENSOR TECHNICAL DATA

HAMAMATSU
TECHNICAL DATA

PCD LINEAR IMAGE SENSORS
S2300 SERIES
(50µm × 5.0 mm Aperture Size)

The S2300 series PCD linear image sensors are monolithic self-scanning photodiode arrays designed specifically for applications in multichannel spectroscopy. The scanning circuit is constructed by a Plasma-Coupled Device (PCD). This scanner is a novel bipolar static shift register and is operatable with a single low power supply voltage. PCD image sensors feature low spike noise, large sensitive areas, and high UV light sensitivity that allow high S/N ratios even in low-light-level detection applications.

The photodiodes of the S2300 series are arrayed in a row with 50 µm center to center spacing and 5.0 mm height. The sensitive area is twice as large as the S2301 series, thus well suited for low-light-level detection requiring high sensitivity. Three different numbers of photodiodes, 256 (S2300-256Q), 512 (S2300-512Q), and 1024 (S2300-1024Q) are available. Quartz glass is the standard window material. (Fiber optic window types are also available.)

From left: S2300-256Q, S2300-512Q, S2300-1024Q, S2300-1024F

FEATURES

- **Wide photosensitive area; 50 µm × 5.0 mm**
- **Bipolar-type image sensor**
- **Wide operating frequency; DC to 2MHz**
- **Operatable with low voltage, single power supply**
- **Logic inputs (start pulse, shift clocks) are TTL compatible (open collector type)**
- **Low capacitive switching noise**
- **High UV sensitivity**
- **High output linearity and uniformity**
- **Low dark current and high saturation charge allow a long integration time for a wide dynamic range even at room temperature.**

IMAGE SENSOR STRUCTURE

The PCD linear image sensor is a monolithic integrated circuit constructed with photodiode arrays, PCD shift register and switching transistors for addressing the photodiodes. Fig.1 shows the equivalent circuit.

The PCD shift register is a static type self-scanner that transfers an addressing pulse along the chain driven by a synchronized three phase clock. Each output pulse (negative polarity) from the PCD shift register is then fed to the base electrode of each p-n-p switch in the video circuit. Photodiodes act as the emitters in these lateral transistors, and operate in the charge storage mode. Therefore the outputs are proportional to the product of the illumination intensity and repeated scanning period.

As shown in Fig.1, the equivalent circuit of S2300 series is very simple, no dummy photodiode is necessary and the signal is available from only one row as a sequential output. Furthermore the uniformity and purity of the signal is high, making it possible to measure the light intensity more accurately with a simple peripheral driving and signal processing circuit.

Fig 2 shows the sensor geometry. The photodiodes consist of diffused p-type regions in n-type silicon substrates. The charges generated in these two regions are collected and stored on the associated P-N junction's capacitance during the integration period. The p-type diffused region is specially processed to have high sensitivity in the UV region and lower dark leakage current.

Figure 1: Equivalent circuit

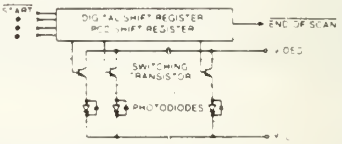
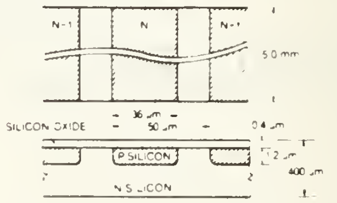


Figure 2: Sensor geometry



MAXIMUM RATINGS

Supply Voltage	10V
Operating Temperature	−30 to +85°C
Storage Temperature	−40 to +125°C

ELECTRICAL CHARACTERISTICS (at 25°)

Parameters	**Symbols**	**S2300-256Q**			**S2300-512Q**			**S2300-1024Q**			**Units**
		Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	
Supply Voltage	Vcc	3	5	7	3	5	7	3	5	7	V
Driving Phase			3			3			3		phase
Shift Pulse Voltage[*1]	Vsh (H)	4.0	5	5.5	4.0	5	5.5	4.0	5	5.5	V
	Vsh (L)			0.8			0.8			0.8	V
Start Pulse Voltage	Vs (H)		Vcc			Vcc			Vcc		V
	Vs (L)			0.8			0.8			0.8	V
Operating Frequency	f	DC		2	DC		2	DC		2	MHz
Photodiode Capacitance	Cp		8			8			8		pF
Video Line Capacitance	Cv		25			40			50		pF
Power Consumption[*1]	P		30			30			30		mW
Photodiode Dark Current[*1]	Id		4	10		4	10		4	10	pA

[*1] At Vcc = 5V

OPTICAL CHARACTERISTICS

Spectral Response (20% of peak)	200 to 1000 nm
Wavelength of Peak Response	600 nm
Saturation Exposure Esat[*1]	50 mlux sec.
Saturation Charge Qsat	37 pC
Sensitivity Uniformity[*2]	within ±5%

[*1] At Vcc = 5V

[*2] 50% of saturation, excluding first element

Figure 3: Typical spectral response

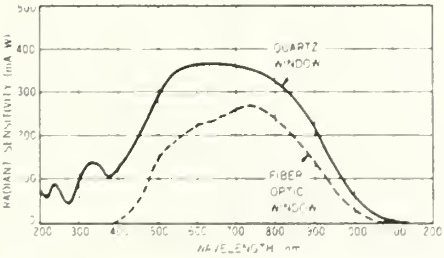


Figure 4. Output charge vs. exposure

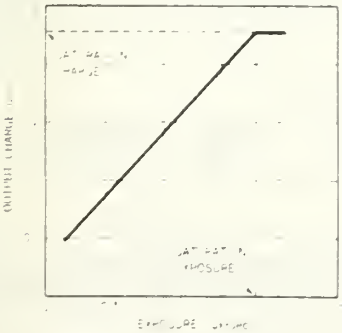
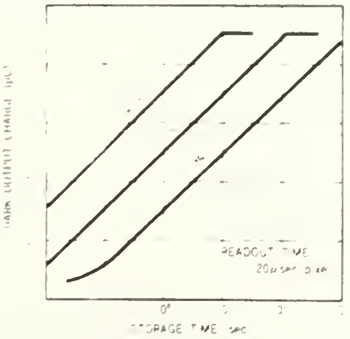
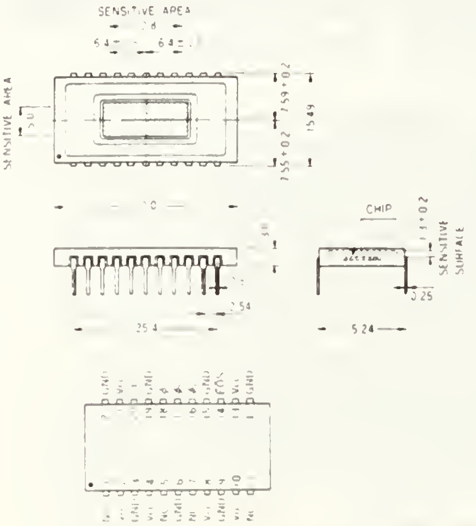


Figure 5: Dark output charge vs. storage time temperature dependency

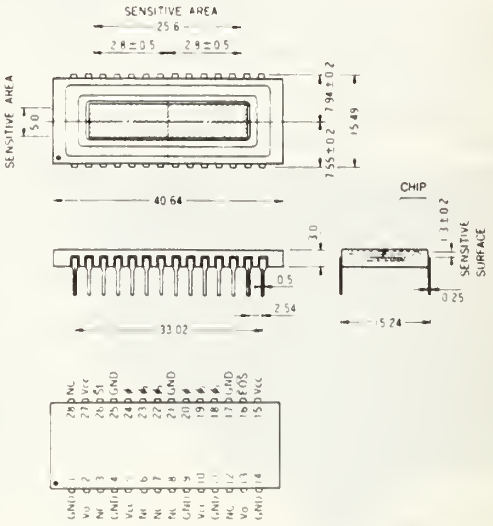


DIMENSIONAL OUTLINES AND PIN CONNECTIONS (Dimensions in millimeters)

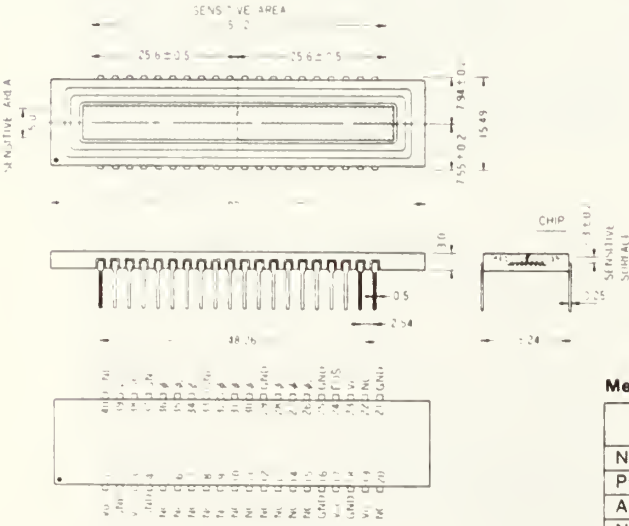
S2300-256Q



S2300-512Q



S2300-1024Q



Symbols	Functions
Vo	Video Output Two Vo are connected inside the element.
Vcc	Power Supply Voltage
GND	Ground (0V)
$\overline{St}$	Start Pulse Input (TTL compatible)
ϕ	Clock Pulse Input (TTL compatible)
$\overline{EOS}$	End of Scan Negative C-MOS compatible. Obtainable at the clock timing just after the last element is scanned
NC	No Connection This should be grounded.

Mechanical Specifications

Parameters	S2300 -256Q	S2300 -512Q	S2300 -1024Q
Number of photodiodes	256	512	1024
Pitch (μm)	50		
Aperture (μm)	50 × 5000		
Number of pins	22	28	40
Window material*	Quartz		
Net weight (g)	4	5	8

*Fiber optic window available.

DRIVING AND AMPLIFIER CIRCUIT

The clock pulse timing and circuit parameter requirments for driving the S2300 series PCD image sensor are shown in Fig.6 and Fig.7. To operate the PCD shift register requires a start pulse to initiate the scan and three phase clock to drive sequentially. The polarity of the start pulse has to be negative and the clock pulses must be positive. These pulses are TTL compatible. The start pulse needs at least 500 ns duration time and a minimum of 200 ns overlap with the clock pulse ϕ_1 to start the scan. It is not always necessary to overlap clock pulses each other, but if a gap of more than 100 ns is presented, scanning will disable.

An open collector type TTL is used to drive the PCD shift register. The voltage level of the start and shift pulse are determined by Vs and Vsh respectively. To provide stable operation of the shift register, it is necessary to select an optimized injection current controlled by resistances R_1 and R_2. Typical values of these driving parameters are shown in Fig.7 and the electrical characteristics table.

To detect low light levels with good linearity, video current integration with a charge-amplifier is recommendable. Fig.7 shows this type of signal extraction with this circuit, the charge-amplifier is reset to ground prior to address each photodiode multiplex switch. When the switch is closed, signal charge flows into capacitors in the integration circuit. The output wave form is a box car shape.

Figure 6: Timing diagram (3-phase drive)

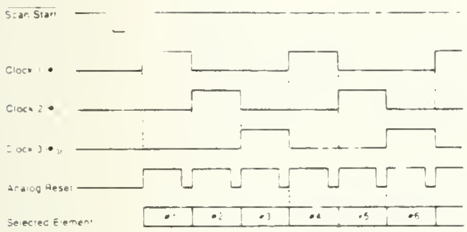
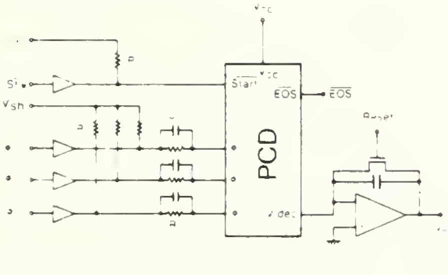


Figure 7: Driving and amplifier circuit



Vcc, Vsh and Vs are operatable with the same supply voltage
Typical values of the parameters
CE. 2 nF, R1 5.6 kΩ, R2 470 Ω

RELATED DEVICES

•S2301, S2304 Series PCD Linear Image Sensors

Hamamatsu provides other sensor geometries for the PCD linear image sensors. The S2301 series has photodiodes of 50 μm × 2.5 mm and the S2304 series has those of 25 μm × 2.5 mm. Types with 128 to 1024 photodiodes are available.

•Driver/Amplifier Circuits for PCD Linear Image Sensors

Driver/amplifier circuits for PCD image sensors are available. These circuits need only a start pulse, master clock pulse, +5V and ± 15V power supply to drive the PCD image sensor. The video output is a voltage output processed by a charge-amplifier. Pulse generator for these driver/amplifier circuits and data processing unit for A/D conversion are also available.

HAMAMATSU
HAMAMATSU PHOTONICS K.K. Solid State Division
1126, Ichino-cho, Hamamatsu City, 435 Japan, Telephone 0534/34-3311 Fax 0534/35-1037 Telex 4225-185

U.S.A. Hamamatsu Corporation, 360 Foothill Road, P.O. Box 6910, Bridgewater, N.J. 08807-0910, Telephone 201-231-0960 Fax 201-231-1539
W. Germany Hamamatsu Photonics Deutschland GmbH, Arzbergerstr. 10, D-8036 Herrsching am Ammersee, Telephone 08152-375-0, Fax 08152-2658
France Hamamatsu Photonics France, 49/51 Rue de la Vanne, 92120 Montrouge, Telephone (1) 46 554 758, Fax (1) 46 55 36 65

JUL/87
T-2000 Printed in Japan

APPENDIX B

HAMAMATSU DRIVER AMPLIFIER TECHNICAL DATA

OPERATING INSTRUCTIONS FOR EVALUATION BOARD

HAMAMATSU PHOTONICS K.K.
SOLID STATE DIV.

SD29-890717-0051201.

OPERATING INSTRUCTIONS FOR EVALUATION BOARD

GENERAL

This is low noise driver/amplifier circuit for Hamamatsu PCD Image Sensors (S2300-512Q,-512F).
The PCD image sensor is a monolithic self-scanning photodiode array. Its scanning circuit is constructed by Plasma-Coupled Device(PCD).
This driver/amplifier circuit provides a scanning pulse "Start" and a three phase clock "ϕ 1, ϕ 2, ϕ 3" to drive the PCD image sensor, and includes a charge-amplifier to output the video signal "Video Data" in the charge integration mode.

FEATURES

- Simple operation; a start pulse, a master clock pulse, +5V and ± 15V required.
- Low noise configuration.
- Structure allows for easy cooling and optical alignment.

SPECIFICATIONS

INPUTS ; Supply voltage: + 5 Vdc at 150mA
+15 Vdc at 25mA
-15 Vdc at 25mA

Start: TTL pulse, positive level sensitive. Minimum duration 500 nsec. Used to initialize the circuit and initiate the shift register in the PCD image sensor.

CLK: TTL pulse, rising edge sensitive. Maximum frequency 250 KHz. Used to syncronize the circuit and the shift register in the PCD image sensor.

OUTPUTS ; Trigger: LS-TTL compatible, positive pulse. Available as a start signal for S/H and A/D conversion (optional).

$\overline{\text{B-EOS}}$: HS-CMOS compatible, negative pulse. Available immediatly after scanning at the last pixel is completed. Can be used as end of A/D aquisition.

Video Monitor: Negative voltage output. This output is the integrated PCD video current signal.

Video Data: Positive voltage output. It is the processed signal of the "Video Monitor".

SETUP PROCEDURE

Setup for the evaluation system is shown in Figure 1.

1) Power supply connection

Power, as specified under specifications, must be supplied to the driver/amplifier citcuit inputs.

2) Pulse generator connection

The "Start" pulse and the "CLK" pulse, as specified under specifications, must be supplied to the driver/amplifier circuit inputs. (C2335 "Hamamatsu Pulse Generator" available and can be connected to the two timing inputs respectively.)
The integration time is preset by the "Start" pulse interval while the readout time of each pixel is preset by a "CLK" frequency.

3) Oscilloscope connection

The "Start" pulse input (from C2325 or other clock) is connected both to the C2325 board and to the EXT. TRIG. input of the oscilloscope.
The "Video Data" signal output is the connected to the input of the oscilloscope.

4) S/H and A/D converter connection (optional)

The "Trigger" pulse output can be used as the logic input of S/H and A/D converter. The "Video Data" signal output is then connected to the analog input of the S/H.

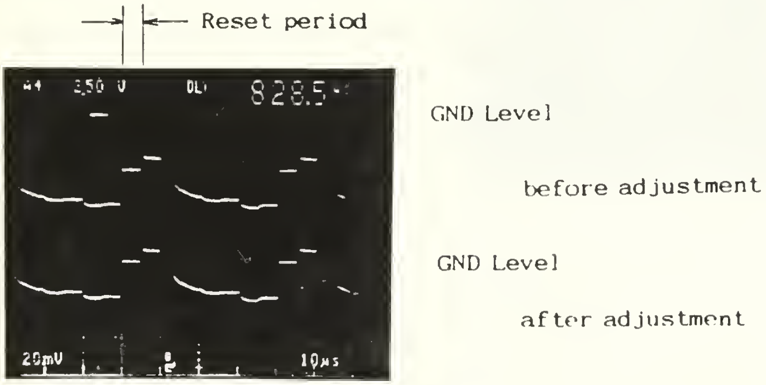
ALIGNMENT PROCEDURE

The driver/amplifier circuit assembly is shown in Figure 2.

REMARK: Use an oscilloscope to monitor the "Video Monitor" or the "Video Data" signal output without any light being illuminated on the photodiode array.

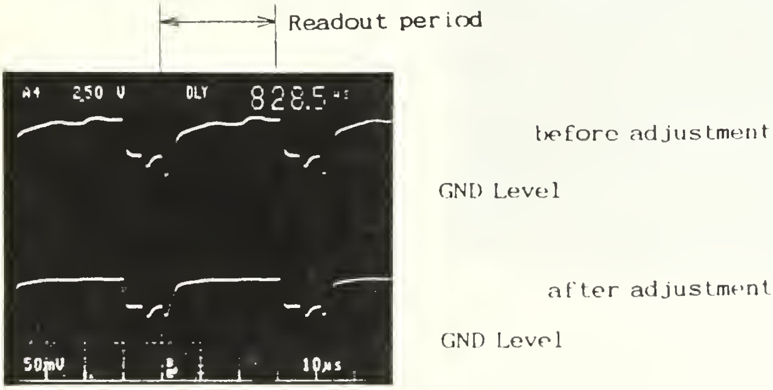
1) Zero level adjustment 1:

Adjust VR2(100K Ω) until the reset level comes to oscilloscope ground level.

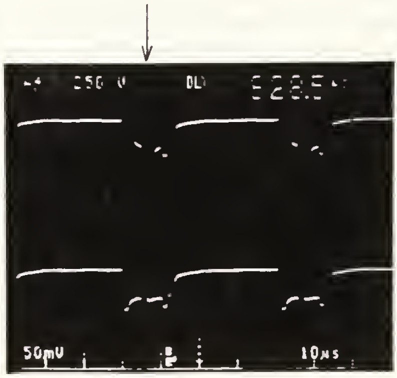


2) Fluctuation (caused by Power supply) cancellation adjustment:

Adjust VR3(1K Ω) until the fluctuation of the "Vedeo Data" signal is minimized.



3) Switching noise cancellation adjustment:
Adjust VR1(10K Ω) until the amplitude of the spike noise is minimized.



before adjustment

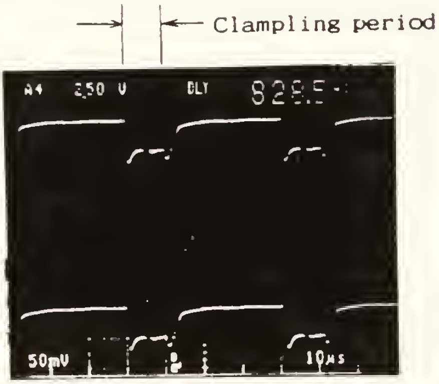
GND Level

after adjustment

GND Level

4) Zero level adjustment 2:

Adjust VR4(10K Ω) until the clampling level comes to oscilloscope ground level.



before adjustment

GND Level

after adjustment

GND Level

REMARKS

If the evaluation system is not operated, regularly check the following items:

1) Are the "Start" pulse and the "CLK" pulse supplied to the driver/amplifier circuit inputs as prescribed under specifications ?

2) Is the scanning pulse "$\overline{\text{Start}}$" supplied to the PCD image sensor ?

3) Is the high level of the three phase clock ($\phi 1$, $\phi 2$, $\phi 3$) according to "Figure 3 Timing Diagram" ?

4) Is the "$\overline{\text{EOS}}$" pulse obtained from the pin of the PCD image sensor ?

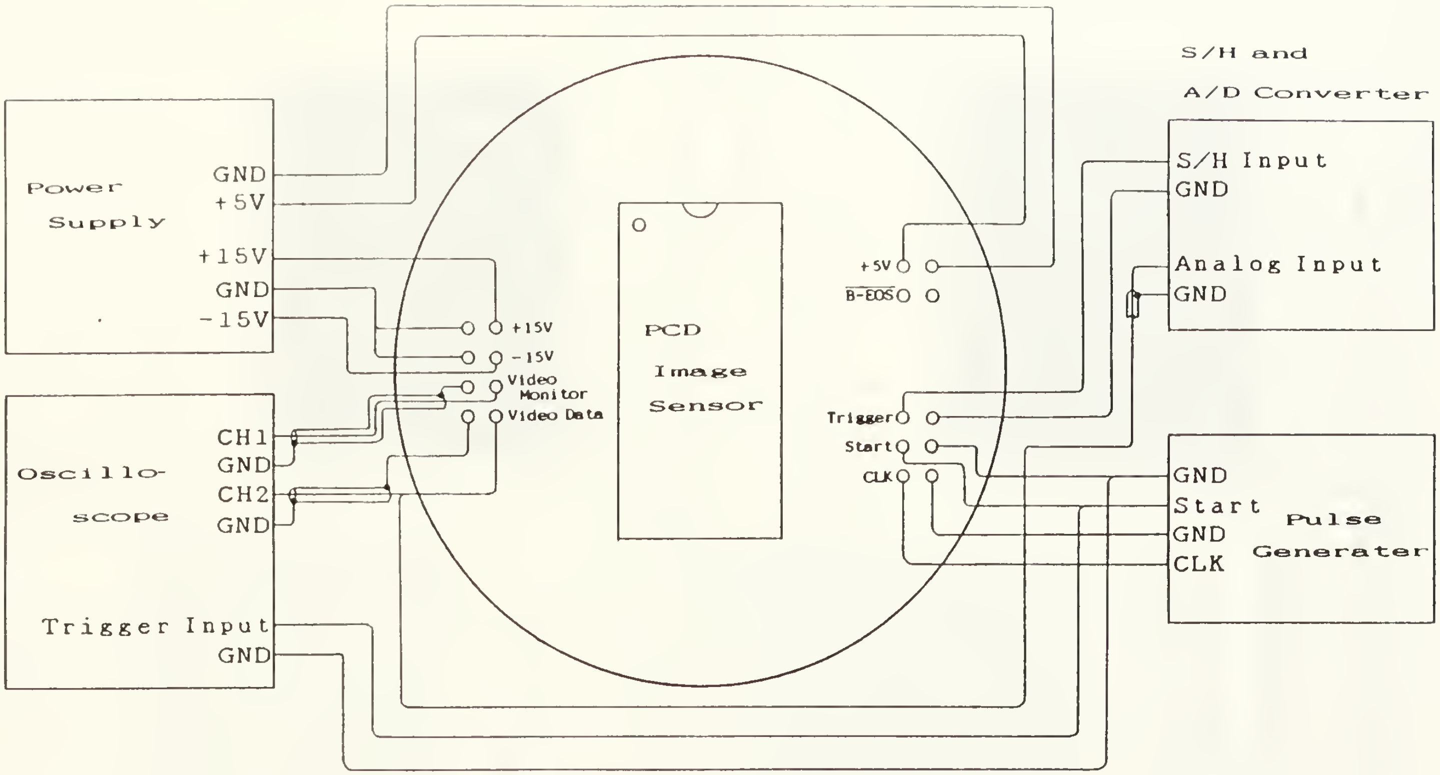
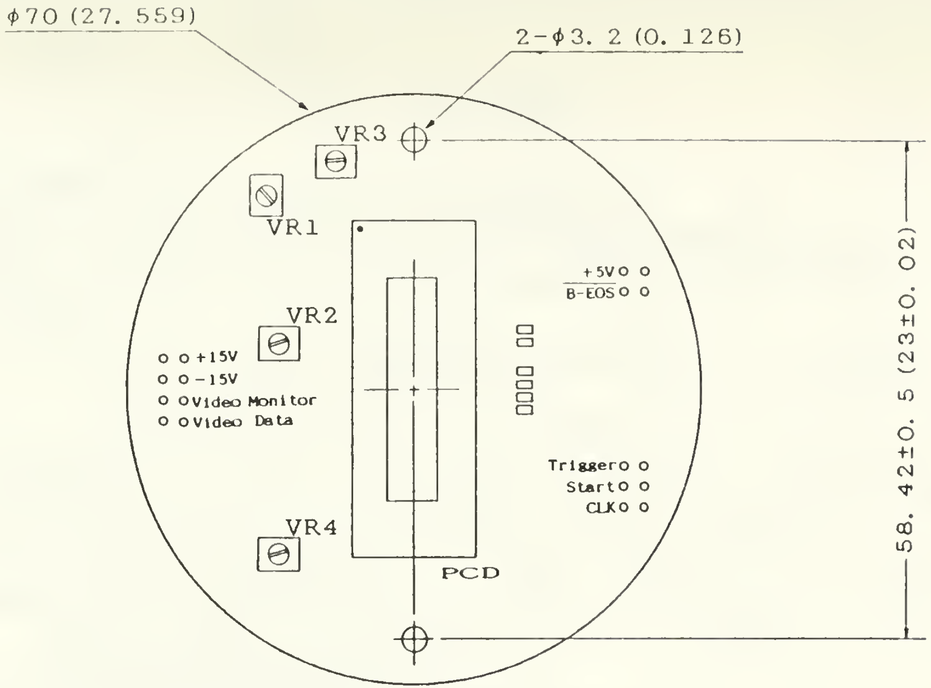
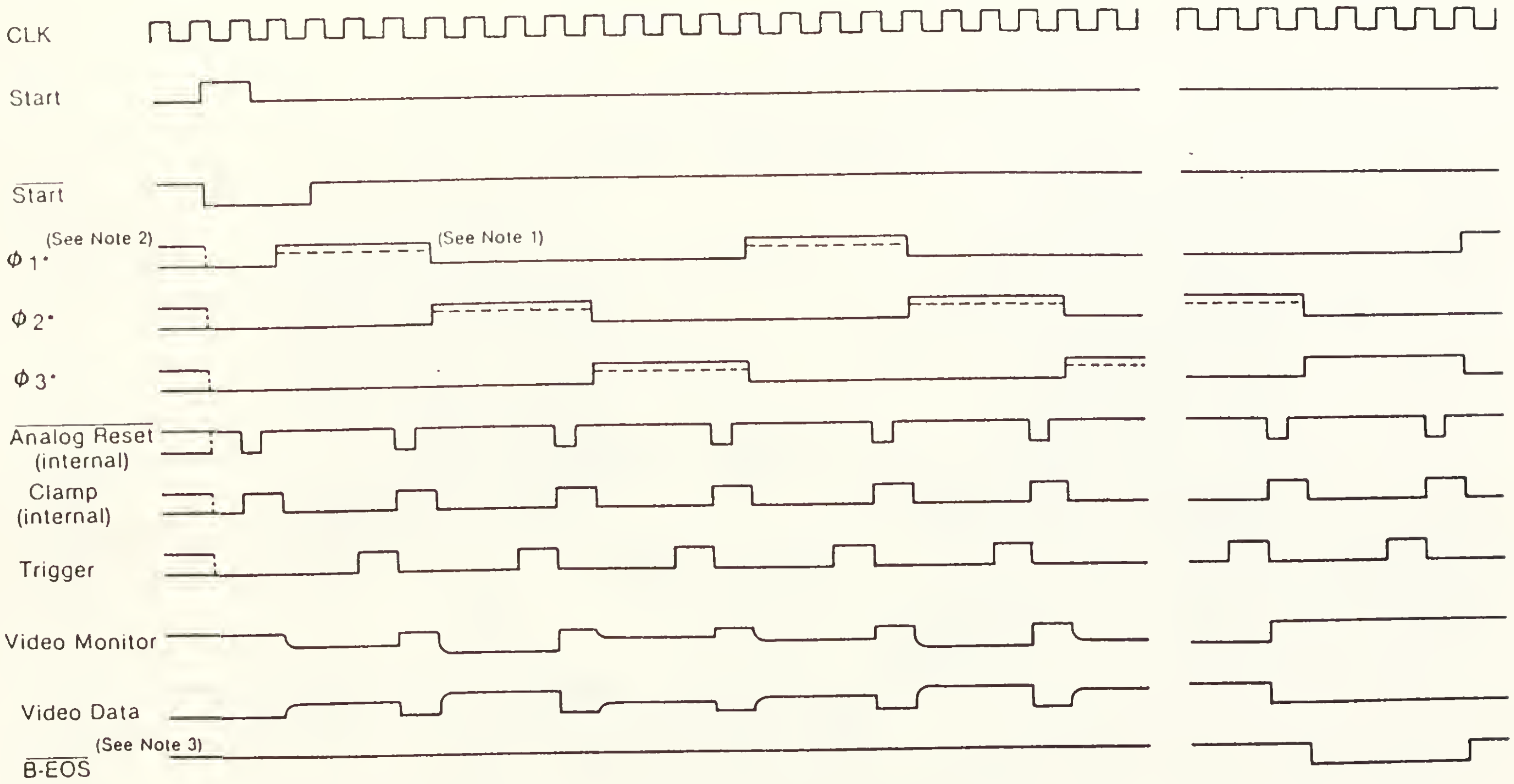


Figure 1   Setup for Evaluation System



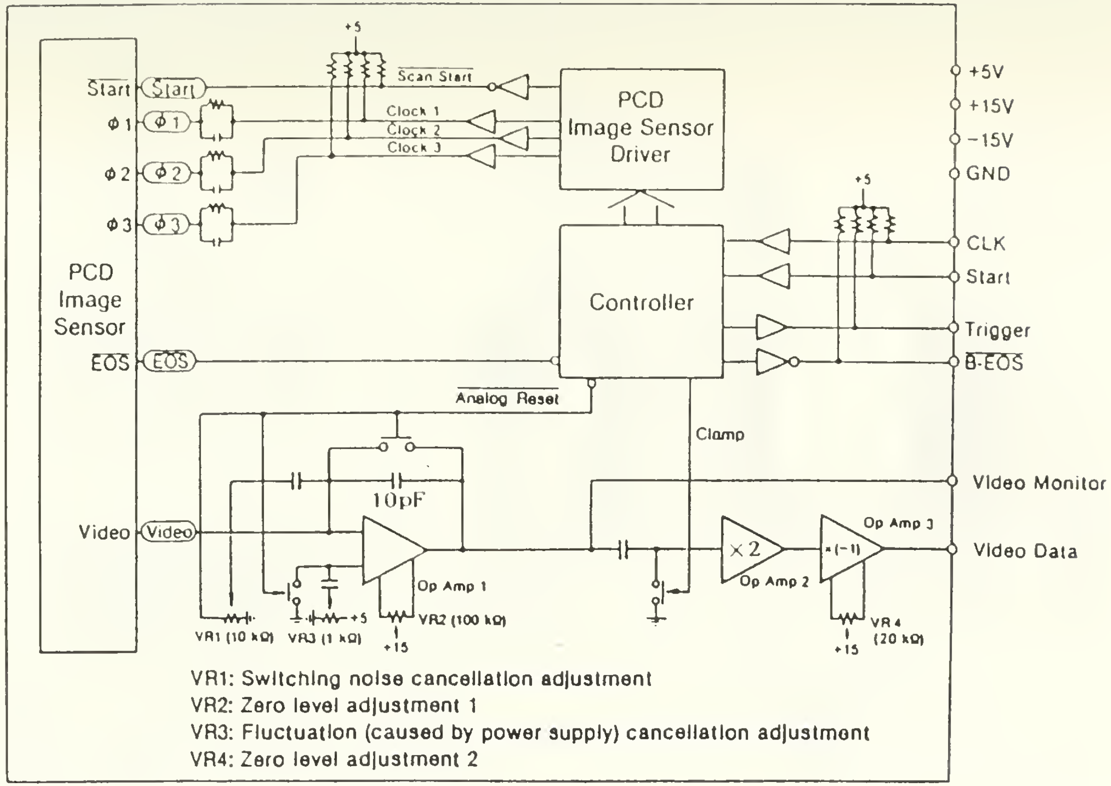
Note: Dimensions in mm (inches)

Figure 2 Board Assembly



Note 1: Solid lines are "PCD-OFF", broken lines "PCD-ON".
2: Pulse width of a three phase clock "Φ1, Φ2, Φ3" is 4 times of a "CLK" period.
3: This $\overline{\text{B-EOS}}$ syncronizes to the next "clock" right after scanning of the last element (of PCD Image Sensors). That is, regarding 128 and 512 elements types, the last element is scanned by Φ2 and $\overline{\text{B-EOS}}$ is obtained by the timing of Φ3. And regarding 256 and 1024 elements types, $\overline{\text{B-EOS}}$ is obtained by Φ2.

Figure 3 Timing Diagram



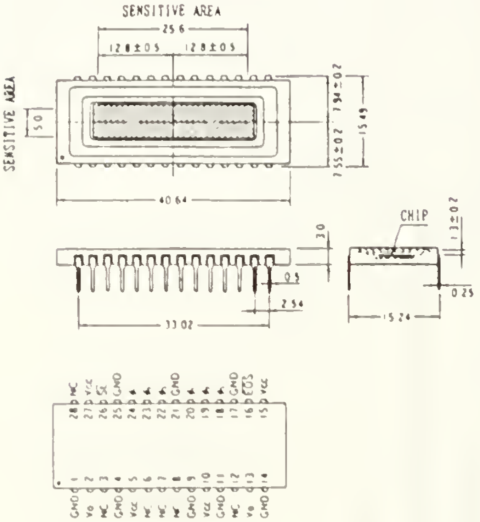
VR1: Switching noise cancellation adjustment
VR2: Zero level adjustment 1
VR3: Fluctuation (caused by power supply) cancellation adjustment
VR4: Zero level adjustment 2

Figure 4 Circuit Configuration

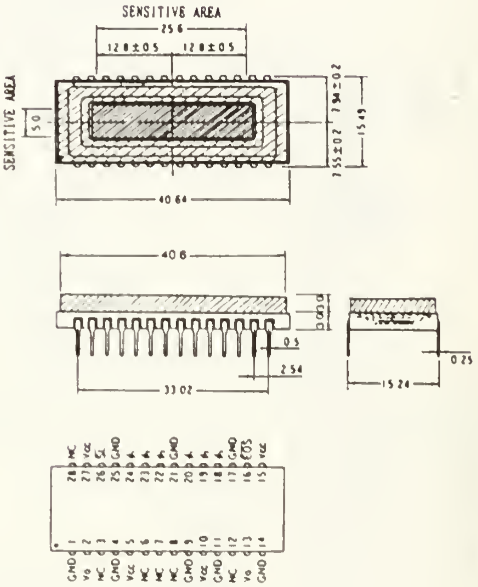
Appendix 1

Pin configurations and package outlines of PCD Image Sensor are shown in Figure A-1

S2300-512Q



S2300-512F



Symbols	Functions
Vo	Video Output Two Vo are connected inside the element
Vcc	Power Supply Voltage
GND	Ground (0V)
$\overline{\mathrm{St}}$	Start Pulse Input (TTL compatible)
ϕ	Clock Pulse Input (TTL compatible)
$\overline{\mathrm{EOS}}$	End of Scan Negative C MOS compatible Obtainable at the clock timing just after the last element is scanned.
NC	No Connection This should be grounded

Parameters	S2300-512Q	S2300-512F
Number of photodiodes	512	
Pitch (μm)	50	
Aperture (μm)	50 x 5000	
Number of pins	28	
Window material	Quartz	Fiber optic plate
Net weight	5g	13.6g

Figure A-1 Pin Configurations and Package Outlines of PCD Image Sensor

Appendix 2

Circuit configuration of the pulse generator is shown in Figure A-2

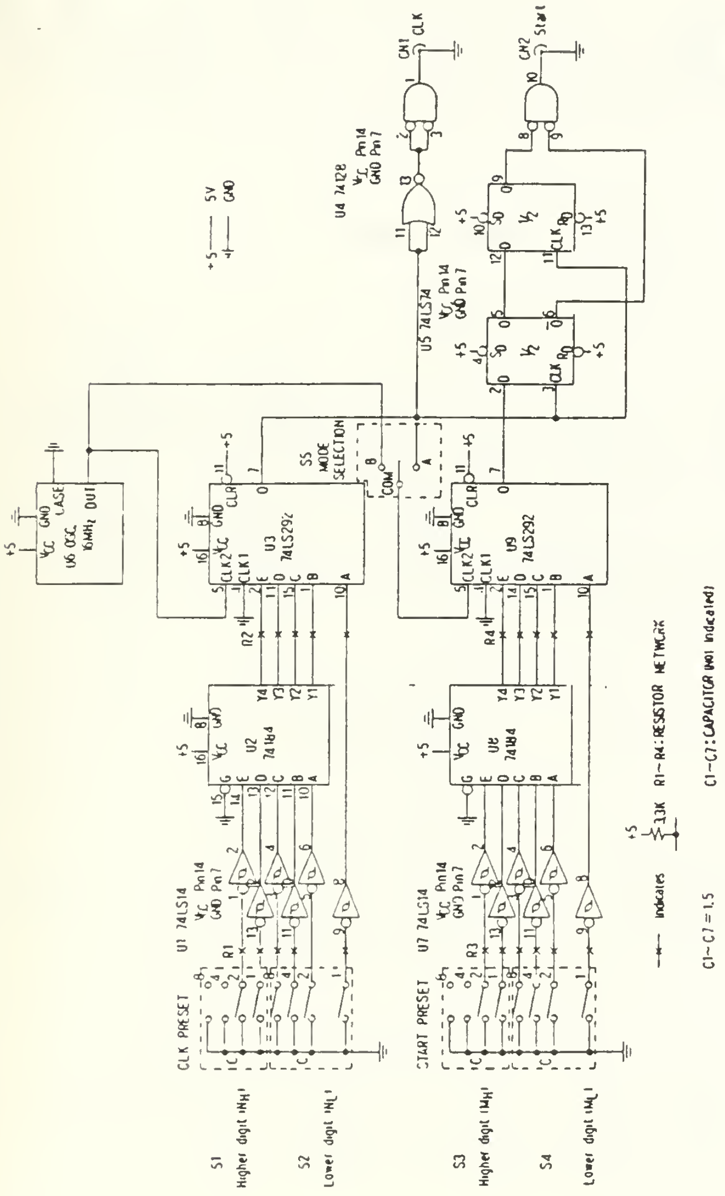


Figure A-2 Circuit Configuration of Pulse Generator

APPENDIX C

POWER SUPPLY TECHNICAL DATA

RSI
RESEARCH SUPPORT INSTRUMENTS, INC
10610 BEAVER DAM ROAD COCKEYSVILLE MARYLAND 21030
PHONE 301-785-6250 FAX 301-785-1228

Item No. 0001AK

LOW VOLTAGE POWER SUPPLY

RSI MODEL 428-211

The RSI Model 428-211 is a low voltage power supply which operates from a nominal +28VDC input. The output of the unit is +5V and provides up to 1000mA. A current limited output monitor is provided in parallel with the output voltage.

The input is series diode protected against inadvertent reversal of the input power lines. Heat sinking of the case is recommended for full power operation.

SPECIFICATIONS:

Input Voltage	+24VDC to +34VDC
Input Current	70mA (no load) 500mA (1000mA load)
Output Voltage	+5V (+-5%)
Output Ripple	< 50mV
Output Spikes	< 75mV
Efficiency	>30% at full load
Converter Frequency	Nominal 10KHz
Operating Temperature	-20 C to +70 C
Storage Temperature	-40 C to +85 C
Line Regulation	.02%/V (no load)

MECHANICAL:

Dimensions	1.0 in.X 3.0 in.X 3.5 in.
Weight	300 grams
Mounting	Four (4) size six clearance holes
Connector	Cannon DAM 15P

OPTIONS:

Voltages other than +5V upon request.
Potting or conformal coating upon request.

Research Support Instruments

Test Report

Low Voltage Power Supply

Model Number 428-211

Serial Number 122503

Voltage Input 28.0 V

Input Voltage (V)	Input Current (mA)	Output Voltage (V)	Output Current (mA)	Monitor Output (V)	Output Ripple (mV)
28	38	5.24	0	5.24	20
28	74	5.23	100	5.23	20
28	108	5.21	200	5.21	25
28	147	5.20	300	5.20	20
28	187	5.18	400	5.18	25
28	224	5.17	500	5.17	25
28	259	5.16	600	5.16	30
28	297	5.14	700	5.14	25
28	337	5.12	800	5.12	25
28	380	5.11	900	5.11	30
28	420	5.09	1000	5.09	30

Notes:

1 Unit should be well heatsunk.
2 Unit loses regulation at 24.2 V input.

Signature Chris Weisner

Date 12-7-89

Disk:wptest File:wp122503.rma

RSI
RESEARCH SUPPORT INSTRUMENTS, INC.
10610 BEAVER DAM ROAD. COCKEYSVILLE. MARYLAND 21030
PHONE 301-785-6250 FAX 301-785-1228

Item No. 0001AL

DUAL TRACKING LOW VOLTAGE POWER SUPPLY

RSI MODEL 441-193

The RSI Model 441-193 is a dual tracking low voltage power supply which operates from a nominal +28VDC input. The outputs of the unit are complementary (+15V and -15V) voltages, each capable of providing 400mA, which track each other under various loads. A current limited output monitor is provided in parallel with the output voltage.

The input is series diode protected against inadvertent reversal of the input power lines. Voltages other than 15V can be supplied upon request. Heat sinking of the case is recommended for full power operation.

SPECIFICATIONS:

Input Voltage	+24VDC to +34VDC
Input Current	70mA (no load) 840mA (400mA load)
Output Voltage	+15VDC @ 400mA -15VDC @ 400mA
Output Ripple	Less than 25mV
Output Spikes	Less than 150mV
Efficiency	60% at full load
Converter Frequency	Nominal 10.5KHz
Operating Temperature	-20 C to +70 C
Storage Temperature	-40 C to +85 C
Line Regulation	0.02%/V (no load)
Load Regulation	0.01%/V (400mA load)

MECHANICAL:

Dimensions	1.0 in.X 3.0 in.X 3.5 in.
Weight	212 grams
Mounting	Four (4) size six clearance holes
Connector	Cannon DAM-15P

OPTIONS:

Voltages other than 15V upon request.
Potting or conformal coating upon request.

Research Support Instruments

Test Report

Low Voltage Power Supply

Model Number 441-193

Serial Number 122508

Voltage Input 28.0 V

Input Current (mA)	Output Voltage (V)		Output Current (mA)		Monitor Output (V)		Output Ripple (mV)	
	+	-	+	-	+	-	+	-
47.7	15.0	15.0	0	0	15.0	15.0	10	10
290	15.0	13.1	0	300	15.0	14.9	10	10
290	13.0	15.0	300	0	14.9	15.0	10	10
536	13.1	13.1	300	300	15.0	14.9	10	10
716	14.9	14.9	400	400	14.9	14.9	10	10

Notes:

1 Unit should be well heatsunk.
2 Unit loses regulation at 25.0 V input.

Signature

Date 11/02/89

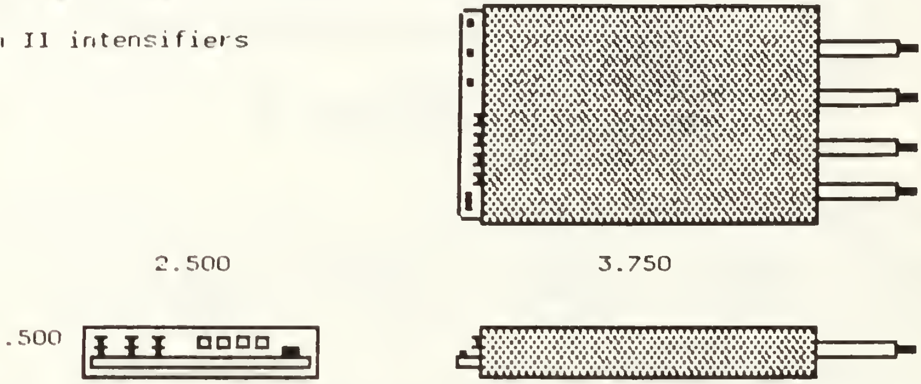
Disk:wptest File:wp122508

RECEIVED OCT - 3 1989

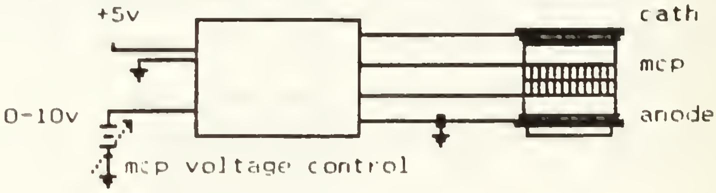
HV POWER SUPPLY GEN II

Grounded Anode

Gen II intensifiers



Model: 200057



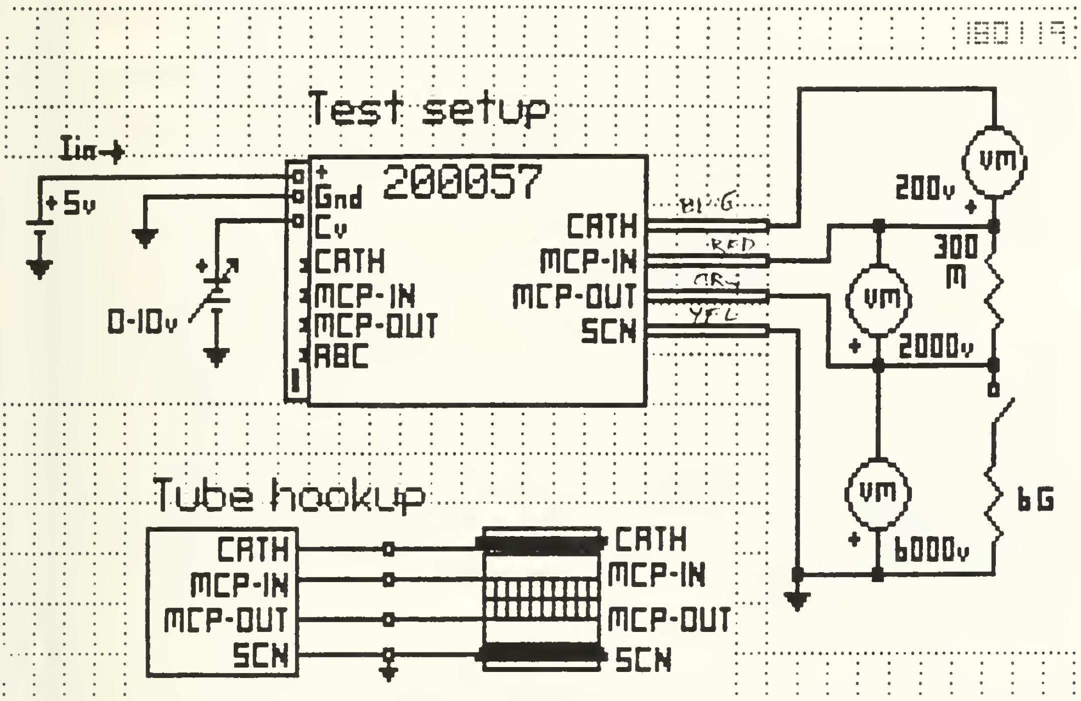
- o Grounded Anode Gen II outputs
- o Adjustable cathode, mcp-in, mcp-out, and ABC level
- o Ext MCP voltage control
- o Ext resistor select - ABC max limit for desired tube dia

cathode voltage	min adjustable range	100 to 240	vdc
	cathode series resistance	1	Gohm
mcp-in voltage	voltage controllable	to 2kv max	vdc
	max load current	20	uA
mcp-out voltage	adjustable	3000 to 6500	vdc
	brightness current limit	.05 to 5	uA
anode output	ground return potential	0	vdc
temperature	operational	- 55 to + 70	C
mechanical	4-40 inserts bottom surface corners		

190079

GBS	NAME Grounded Anode Gen II				DWG NUM 200057	
	SIZE A	BY GBS	DATE 07-27-86	SCALE N/A	REV B	SHT 1 OF 1

PS 200057 Test Data Sheet



Test Data at Delivery S/N : 010 Date : 7-13-87 By : C.is

Parameter	Data	Units
1. Cathode voltage @ no load	200	- VDC
Cathode voltage @ 1M	1.5	- VDC
2. Mcp-in voltage @ 300M @ Cv=10v	1700	- VDC
8v	1400	- VDC
6v	1100	- VDC
4v	700	- VDC
2v	270	- VDC
3. Mcp-out voltage @ no load	5500	- VDC
@ 1 uA load	5450	- VDC
4. Rabc set value	1.0	megohm
ABC adj pot set for I-limit of	1.0	uA
5. Input current @ +5vdc @ ss	87	mADC
6. Burn-in	48	hrs
7. Mechanical and visual	✓	check

90126

GBS	NAME PS 200057 Test Data Sheet			DWG NUM 200123	
	SIZE A	BY GBS	DATE 02-16-87	SCALE N/A	REV A	SHT 1 OF 1

Operation and Instructions
PS 200057 grounded anode standard GEN II

1.0 General

The model 200057 power supply is a small DC to DC converter which converts +5 vdc to multiple HV dc outputs for use by a Gen II image intensifier tube. The outputs are line regulated, and each is independently adjustable. The power supply circuitry is fully potted in an RTV encapsulant due to the high internal voltages generated, and due to the small size of the power supply.

Manufacturer : GBS Micro Power Supply
6155 Calle Del Conejo
San Jose, California 95120
408-997-6720

2.0 Power Supply Inputs

The following inputs are available and marked on the power supply.

1. Input voltage terminal	+5 +-.5 vdc
2. Input voltage return terminal (gnd)	
3. Voltage control terminal	0 to +10 vdc
4. Cathode output adj pot	
5. MCP-IN output adj pot	
6. MCP-OUT output adj pot	
7. ABC limit fine adjust pot	
8. Rsel resistor for gross ABC limit adj	

3.0 Output Connections

There are 4 output leads for connection to the image intensifier.

1. Cathode output	typically -175 vdc with respect to the MCP-IN output lead
2. MCP-IN output	typically -1500 vdc with respect to the MCP-OUT output lead
3. MCP-OUT output	typically -6000 vdc with respect to the screen output lead
4. Screen output	Gnd, and tied to the +5 return internally in the power supply.

4.0 Voltage Control

The MCP voltage applied to the intensifier, is provided by the MCP-IN and MCP-OUT outputs, which is termed the MCP voltage. This voltage can be remotely varied from approximately -400 vdc, (the oscillator drop out level), to -2000 vdc, by varying the voltage applied to the voltage control terminal from 0 to +10 vdc. The +10 vdc results in -2000 vdc MCP voltage. An open at the voltage control terminal results in a 0 vdc MCP voltage.

90123

GBS	NAME PS 200057 Operation & Instructions				DWG NUM 200122	
	SIZE A	BY DH	DATE 4-17-88	SCALE N/A	REV A	SHT 1 OF 3

FORM F15001

The -2000 vdc MCP voltage when the control voltage is at +10 vdc, can be lowered to near -400 vdc by adjusting the MCP-IN adjust pot counter clockwise. CW increases MCP voltage toward -2000. CCW reduces MCP voltage toward 0 vdc.

5.0 Cathode Output

The cathode output is adjustable via a trim pot. CW increases the output to -250 vdc. CCW reduces the output to -100 vdc. A cathode current limiting resistor (1 Gigohm) is internal in the power supply, and will drop the cathode voltage as excess tube cathode current is developed in high illumination conditions. When the cathode current, under these high current conditions, falls to approximately -3 vdc with respect to the MCP voltage, a diode in the power supply, shunts the 1 Gigohm limit resistor, with a 22 Megohm resistor, thereby extending the cathode current availabe, before eventual tube cutoff. The cathode output is typically -175 vdc with respect to the MCP-IN output, but it is stacked on the other power supply outputs, so that with respect to ground, the potential on the cathode lead is approximately -8000 vdc. This high voltage is usually a source of trouble when operating the power supply, as leakage to gnd may often readily develop. This leakage will be treated by the power supply as ABC current, which is an instruction to the power supply to lower, or shut off the MCP-IN voltage. Caution is recommended in the testing of the power supply, and in the tube connections.

6.0 MCP-out Voltage

The MCP-out is the votage provided for the intensifier screen, and is -6000 vdc typically. This output is connected to the MCP-OUT intensifier lead. CW adjustment of the trim pot increases this voltage to -6500 vdc. CCW decreases the voltage to -3000 vdc. This high voltage is developed in the power supply by a stack of voltage doubler circuits. This multiplier circuit is resistor returned to gnd, so that any tube screen current flowing at any time, must pass through the resistor. A voltage is developed across the resistor, and is proportional to the tube screen current. The voltage developed, is compared to an ABC limit setting, and will shut down the MCP voltage to the tube, if the threshold level is reached.

7.0 ABC

The R-select resistor (externally available as Rsel), is used to sense the tube screen current as described in paragraph 6.0. The power supply comparator for ABC, has a threshold level of 1 vdc and will shut down the MCP voltage when the Rsel voltage reaches this 1 vdc threshold. The choice of resistance for Rsel, then can determine at what tube current, shutdown is desired. Typically, Rsel is chosen as 1 Megohm, so that it allows ample current for normal tube use, but limits screen current to a maximum of 1 uA.

90119

GBS	NAME PS 20057 Operation & Instructions				DWG NUM 208122	
	SIZE A	BY DH	DATE 4-19-88	SCALE N/A	REV A	SHT 2 OF 3

FORM F15001

The ABC trim pot allows fine resolution of the threshold voltage used by the shutdown comparator. CW increases the threshold to 1.0 vdc. CCW decreases the threshold voltage to 0 vdc. In this manner, the ABC pot can be used to fine tune the limit current circuitry for use as an automatic brightness control feature, (ABC).
The power supply has a 22 Megohm internal resistor in parrallel with the external Rsel.
At delivery, Rsel is set to 1 Megohm, and the ABC pot is adjusted for so that 1 uA of screen current reduces the MCP voltage 50%.

8.0 Mechanical, Leads

The power supply chassis is glass epoxy with TRV potting internal.
There are 4 Mounting inserts on the base of the power supply, 4-40 inserts.
The output leads are silicone coated teflon insulated stranded wires, reated for 15kv.

9.0 Processing, Burn-in

Standard processing prior to delivery includes 24 hrs of operation unpotted, at 23C, at nominal output voltage levels, followed by 48 hrs of operation at 23C, at typical output voltage levels, followed by a final electrical performance test at 23C.
Other tests and burn-in environments may be conducted as specified by the customer purchase order.

10.0 Test Circuitry

Electorstatic voltmeters or equivalent high input impedance (> 300 Gigohm) divider probes are recommended when checking output voltage levels.
A dc voltage applied to Rsel can be used to simulate tube screen current for MCP shutdown verification. This voltage should not exceed 5 vdc, the input supply voltage.

90119

GBS	NAME PS 200057 Operation & Instructions				DWG NUM 200122	
	SIZE A	BY DH	DATE 4-12-88	SCALE N/A	REV A	SHT 3 OF 3

APPENDIX D

ANALOG TO DIGITAL CONVERTER TECHNICAL DATA

(HAS1202A MB)

ANALOG
DEVICES

Ultrafast Hybrid Analog-to-Digital Converters

HAS-1202/HAS-1202A

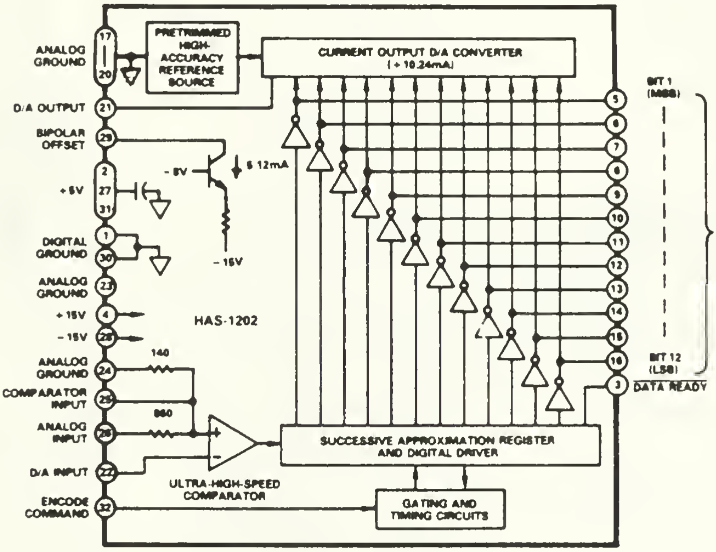
FEATURES

- **Conversion Time of 1.56μs (HAS-1202A)**
- **12-Bit Resolution**
- **Conversion Rates to 641kHz**
- **Adjustment-Free Operation**

APPLICATIONS

- **Waveform Analysis**
- **Fast Fourier Transforms**
- **Radar Systems**

HAS-1202 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HAS-1202 and improved HAS-1202A A/D converters are thick-film hybrid 12-bit converters housed in 32-pin ceramic or metal DIP packages. They can be used with high-performance track-and-hold (T/H) amplifiers to solve high-speed, high-resolution digitizing problems economically and feature conversion times of 2.86μs (HAS-1202) and 1.56μs (HAS-1202A).

These converters and the Analog Devices Model HTC-0300A T/H offer designers an opportunity to go from analog to digital with savings in power, board space, design time, and component costs.

They are ideally suited for applications which require excellent performance with a minimum of adjustments. Included in these potential uses are radar systems, PCM, data acquisition systems, and digital signal processing (DSP) systems of various kinds.

The HAS-1202 and HAS-1202A are rated over an operating temperature range of 0 to +70°C and are packaged in 32-pin DIP ceramic housings. The HAS-1202M and HAS-1202AM are rated over a range of −55°C to +85°C and are packaged in metal cases. For metal case units with an operating range of −55°C to +100°C and military screening, order part numbers HAS-1202MB or HAS-1202AMB. Their performance characteristics are identical except for differences in conversion rates; the HAS-1202 is specified for a maximum rate of 349kHz, while the HAS-1202A is capable of operating up to 641kHz.

SPECIFICATIONS (typical @ + 25°C with nominal power supplies unless otherwise noted)

	HAS-1202A	HAS-1202
MAXIMUM RATINGS		
Positive Supply (Pin 4)	+ 16VDC	•
Negative Supply (Pin 28)	− 16VDC	•
Logic Supply (Pins 2, 27, 31)	+ 7VDC	•
Analog Input (Pin 26)	20V	•
Logic Input	+ 7V	•
(Encode Command @ Pin 32)		
Temperature		
Operating (Case)	− 55°C to + 100°C	•
Storage	− 55°C to + 125°C	•

Parameter	Units	HAS-1202A	HAS-1202
RESOLUTION (FS = Full Scale)	Bits (%FS)	12 (0 025)	•
LEAST SIGNIFICANT BIT (LSB) WEIGHT	mV	2.5	•
ACCURACY			
Monotonicity		Guaranteed	•
Integral Nonlinearity	LSB	± 1/2	•
Differential Nonlinearity	LSB	± 1/2	•
Nonlinearity vs. Temperature	ppm/°C	3.5	•
Gain Error	%FS, max	0.08 (0 18)	•
Gain vs. Temperature	ppm/°C	60	•
Gain vs. Power Supply Changes	ppm/mV	2.2	•
DYNAMIC CHARACTERISTICS			
Conversion Rate	kHz, max	641	349
Conversion Time[1]	µs, max	1.56	2.86
vs. Temperature	%/°C	0.08	•
ANALOG INPUT			
Voltage Ranges			
Bipolar	V	± 5.12	•
Unipolar	V	0 to + 10.24	•
Overvoltage	V, max	20	•
Impedance	Ω, max	1,000 (± 20)	•
Offset[2]			
Initial	mV, max	7 (38)	•
vs. Temperature			
Unipolar Input	ppm/°C	7	•
Bipolar Input	ppm/°C	35	•
ENCODE COMMAND INPUT[3]			
Logic Levels, TTL-Compatible	V	"0" = 0 to + 0.4 "1" = + 2 4 to + 5	• •
Impedance	TTL Loads	1 "S" and 1 "LS"	•
Rise and Fall Times	ns, max	10	•
Width			
Min	ns	50	•
Frequency	kHz	dc to 641	dc to 349
DIGITAL OUTPUT			
Format	Data Bits	12 Parallel, NRZ	
	$\overline{\text{Data Ready}}$	1; RZ	•
Logic Levels, TTL-Compatible	V	"0" = 0 to + 0 4 "1" = + 2 4 to + 5	• •
Drive	TTL Loads	5 Standard	•
Coding		Binary (BIN) Offset Bin. (OBN)	
POWER REQUIREMENTS			
+ 15V ± 0.5V	mA (max)	48 (60)	•
− 15V ± 0.5V	mA (max)	30 (46)	•
+ 5V ± 0.25V	mA (max)	150 (232)	•
Power Dissipation	W, max	1.9 (2.75)	•
TEMPERATURE RANGE[4]			
Operating	°C	0 to + 70	•
NOTE For operating range of − 25°C to + 85°C, specify HAS-1202M or HAS-1202AM, for operating range of − 55°C to + 100°C and military screening, specify HAS-1202MB or HAS-1202AMB.			
THERMAL RESISTANCE[5]			
Junction to Air, θ_{JA} (Free Air)	°C/W	38	•
Junction to Case, θ_{JC}	°C/W	18	•
PACKAGE OPTION[6]			
M-32		HAS-1202A	HAS-1202

For applications assistance, call Computer Labs Division @ (919) 668-9511.

NOTES

*Specifications same as HAS-1202A

[1] Measured from leading edge of Encode Command to trailing edge of $\overline{\text{Data Ready}}$ with 50ns encode pulse Conversion time increases equally with increasing width of Encode Command

[2] Externally adjustable to zero

[3] Transition from digital "0" to digital "1" initiates encoding

[4] Case temperature Metal case HAS-1202M/HAS-1202AM have operating ranges of − 25°C to + 85°C, HAS-1202MB/HAS-1202AMB have operating ranges of − 55°C to + 100°C and military screening

[5] Maximum junction temperature = 150°C

[6] See Section 14 for package outline information

Specifications subject to change without notice

HAS-1202/HAS-1202A PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
32	ENCODE COMMAND	1	DIGITAL GROUND
31	+ 5V	2	+ 5V
30	DIGITAL GROUND	3	$\overline{\text{DATA READY}}$
29	BIPOLAR OFFSET	4	+ 15V
28	− 15V	5	BIT 1 (MSB)
27	+ 5V	6	BIT 2
26	ANALOG INPUT	7	BIT 3
25	COMPARATOR INPUT	8	BIT 4
24	ANALOG GROUND	9	BIT 5
23	ANALOG GROUND	10	BIT 6
22	D/A INPUT	11	BIT 7
21	D/A OUTPUT	12	BIT 8
20	ANALOG GROUND	13	BIT 9
19	ANALOG GROUND	14	BIT 10
18	ANALOG GROUND	15	BIT 11
17	ANALOG GROUND	16	BIT 12

NOTE

Analog Ground (Pins 17-20; 23; 24) and Digital Ground (Pins 1 and 30) Are Electrically Independent of Each Other. Connect Together Externally and to Low-Impedance Ground Plane as Close to Device as Possible.

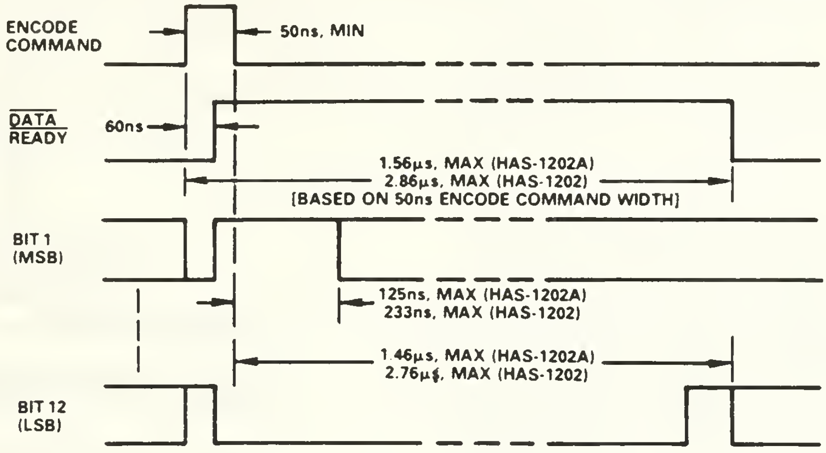


Figure 1. HAS-1202 1202A Timing Diagram

HAS-1202 TIMING

Refer to Figure 1, HAS-1202/1202A Timing Diagram.

The TTL-compatible Encode Command pulse (applied to Pin 32) has a minimum width of 50 nanoseconds. As the width of the Encode Command is increased from this minimum, the width of the $\overline{\text{Data Ready}}$ pulse (and the conversion time) is increased by an equal amount. For the HAS-1202, maximum encode frequency is 349kHz; for the HAS-1202A, maximum encode rate is 641kHz.

When the leading edge of the encode signal arrives, data outputs resulting from the preceding encode command will be at their previous values; the $\overline{\text{Data Ready}}$ pulse, being RZ, will be at a digital "0" logic level.

The $\overline{\text{Data Ready}}$ pulse will typically transition from digital "0" to digital "1" 60 nanoseconds after the leading (positive-going) edge of the Encode Command. It will remain at logic "1" until all data outputs have established levels indicative of the input analog value which is present during the conversion period.

As expected, and as shown in Figure 1, the length of the $\overline{\text{Data Ready}}$ pulse and the corresponding availability of digital output data are different for the two models of HAS-1202 converters because of their differences in speed capabilities.

CALIBRATION PROCEDURE

Input connections for the HAS-1202 and HAS-1202A A/D Converters are shown in Figure 2.

The values for resistors R_A, R1, and R2 in the Gain Adjust portion of Figure 2 are a function of the desired analog input range.

For full-scale inputs ≥10.496 volts:

$R1 = (\text{FS p-p} \times 97.66) - 1050$
R2 = Not used
$R_A = 100\Omega$

For full-scale inputs <10.496 volts:

$R1 = 0\Omega$

$$R2 = 860\left[\frac{(\text{FS p-p} \times 97.66) - 165}{1025 - (\text{FS p-p} \times 97.66)}\right]$$

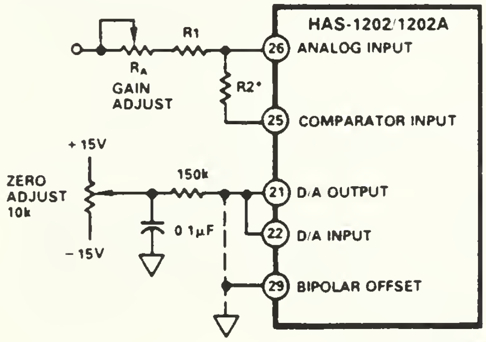
$R_A = 50\Omega$

The dotted lines between Pins 21 and 29 and ground in Figure 2 are used to show differences in connections for unipolar and bipolar modes. For unipolar, ground Pin 29; for bipolar, connect Pins 21, 22, and 29 together without grounding.

When calibrating for either unipolar or bipolar operation, an encode command at a frequency of 200kHz should be applied to Pin 32. Zero Adjust must always be adjusted before Gain Adjust, no matter which mode of operation is being calibrated.

Connect a precision voltage reference source between the analog input and ground.

If the converter is to be operated in a unipolar mode, adjust the output of the voltage reference to the desired full-scale positive input voltage, as described in Table I. After adjusting the Zero Adjust control per the directions in Table I, reset the reference and calibrate Gain Adjust.



*NOT USED FOR INPUTS ≥10.496V

Figure 2. Gain and Offset Adjust

UNIPOLAR INPUT CALIBRATION
(For **Analog Input Range** 0V to + **Full-Scale**)

Apply Reference	And Adjust	For "Dither" Between
$+FS \times (1.22 \times 10^{-4})$	Zero	0 000 000 000 and 0 000 000 001
$+FS \times (0.99963)$	Gain	1 111 111 110 and 1 111 111 111

Table I.

If the converter is to be operated in a bipolar mode, refer to Table II.

BIPOLAR INPUT CALIBRATION
(For **Analog Input Range** − **FS** to + **FS**)

Apply Reference	And Adjust	For "Dither" Between
$-FS \times (0.99976)$	Zero	0 000 000 000 and 0 000 000 001
$+FS \times (0.99927)$	Gain	1 111 111 110 and 1 111 111 111

Table II.

Note that Zero Adjust is set using the negative input voltage for bipolar operation, while Gain Adjust is calibrated with the positive bipolar input.

USING HAS-1202 WITH TRACK/HOLD

Figure 3 and Figure 4 illustrate possible combinations of the HAS-1202 or HAS-1202A A/D Converter with the HTC-0300A Track-and-Hold amplifier.

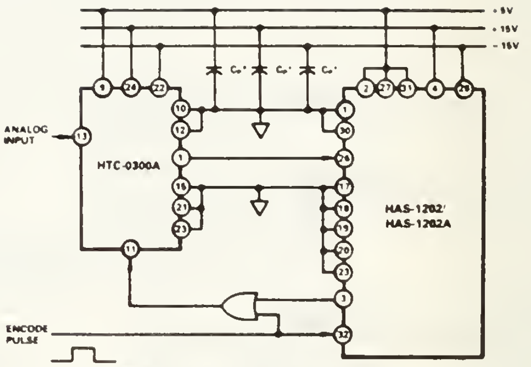
As shown, the upper word rate of the combination will be a function of which converter is used. When comparing the maximum word rates shown in the Specifications Table and the ones shown in the illustrations, there seems to be a disparity in encode rate capabilities.

The word rates shown in Figures 3 and 4, however, are correct and are based on "real-life" circuits using a T/H. The T/H needs sufficient time to acquire and/or settle to 12-bit accuracy. This interval is longer than the conversion time of the HAS-1202, and the result is a lower word rate for the combination than that which is possible with only the converter.

Note in Figure 3 that the encode pulse is applied, via an OR gate, to the ENCODE COMMAND input of the HTC-0300A. In Figure 4, it is applied directly to the ENCODE COMMAND input.

Circuit layout is extremely critical in using a high-speed converter and T/H to accomplish digitizing of analog signals; this is especially true with 12-bit systems of the type shown here.

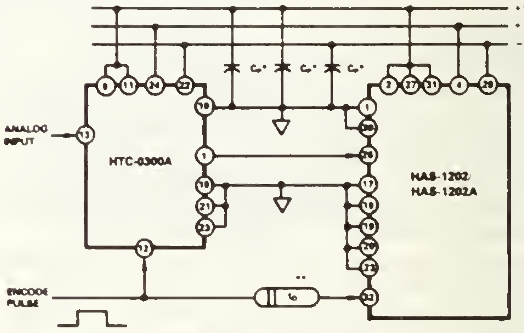
In this context, "circuit layout" encompasses all of the important items which need to be considered. This includes, but is not limited to, precautions such as establishing low-impedance grounds; careful routing of analog and digital signal paths to avoid interference; and keeping all signal paths as short as possible. Bypassing of all power supplies is mandatory for best performance.



*C_p ARE TANTALUM CAPACITORS OF 1-10µF
ALL POWER SUPPLIES SHOULD ALSO BE BYPASSED
WITH 0.1µF CERAMIC CAPACITORS CONNECTED
DIRECTLY TO PIN

MODEL	ENCODE PULSE WIDTH (MIN.)	ENCODE FREQ. (MAX.)
HAS-1202	100ns	322kHz
HAS-1202A	100ns	562kHz

Figure 3. 12-Bit A/D Conversion System



*C_p ARE TANTALUM CAPACITORS OF 1-10µF
ALL POWER SUPPLIES SHOULD ALSO BE BYPASSED
WITH 0.1µF CERAMIC CAPACITORS CONNECTED
DIRECTLY TO PIN

**t_D CAN BE DECREASED (OR REMOVED) BUT MAY
DEGRADE PERFORMANCE. AMOUNT OF DEGRADATION
HEAVILY DEPENDENT ON CIRCUIT LAYOUT

MODEL	**t_D (MIN.)	ENCODE PULSE WIDTH (MIN.)	ENCODE FREQ. (MAX.)
HAS-1202	40ns	250ns	320kHz
HAS-1202A	80ns	250ns	500kHz

Figure 4 12-Bit A/D Conversion System

For optimum performance in noisy environments, 2k pulldown resistors should be connected to Bits 1 through 4.

ORDERING INFORMATION

With the exception of conversion rates, the specifications are the same for the HAS-1202 and HAS-1202A A/D Converters; both units are housed in 32-pin DIP ceramic packages. For metal case versions with extended temperature ranges of −25°C to +85°C, order model number HAS-1202M or HAS-1202AM. For metal case versions with extended temperature ranges of −55°C to +100°C and military screening, order model number HAS-1202MB or HAS-1202AMB. Consult factory for details.

APPENDIX E

DIGITAL TO ANALOG CONVERTER TECHINCAL DATA

(AD667SD)

ANALOG
DEVICES

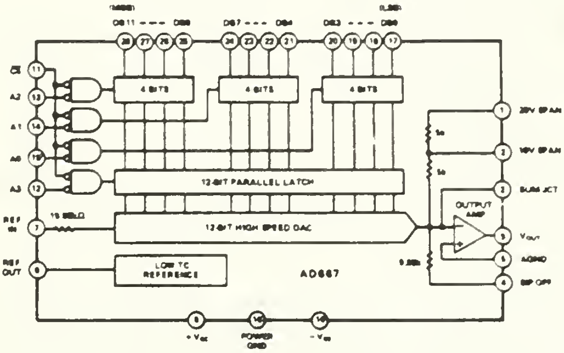
Microprocessor-Compatible 12-Bit D/A Converter

AD667*

FEATURES

- **Complete 12-Bit D/A Function**
  - **Double-Buffered Latch**
  - **On Chip Output Amplifier**
  - **High Stability Buried Zener Reference**
- **Single Chip Construction**
- **Monotonicity Guaranteed Over Temperature**
- **Linearity Guaranteed Over Temperature: 1/2LSB max**
- **Settling Time: 3μs max to 0.01%**
- **Guaranteed for Operation with ±12V or ±15V Supplies**
- **Low Power: 300mW Including Reference**
- **TTL/5V CMOS Compatible Logic Inputs**
- **Low Logic Input Currents**

AD667 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD667 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD667 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD667 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K, B grades) at 25°C and ±1/2LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity, is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD667 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 5ppm/°C.

The AD667 is available in five performance grades. The AD667J and K are specified for use over the 0 to +70°C temperature range and are available in a 28-pin molded plastic DIP (N) or PLCC (P) package. The AD667S grade is specified for the −55°C to +125°C range and is available in the ceramic DIP (D) or LCC (E) package. The AD667A and B are specified for use over the −25°C to +85°C temperature range and are available in either a 28-pin hermetically sealed ceramic DIP (D) or LCC (E) package.

PRODUCT HIGHLIGHTS

1. The AD667 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried Zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain setting and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current steering switch and on-board high speed output amplifier settle within 1/2LSB for a 10V full scale transition in 2.0μs when properly compensated

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*Covered by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending

SPECIFICATIONS (T_A = +25°C, ±12V, ±15V power supplies unless otherwise noted)

Model	AD667J			AD667K			
	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS							
Resolution			12			12	Bits
Logic Levels (TTL Compatible, T_{min}–T_{max})[1]							
V_{IH} (Logic "1")	**+2.0**		+5.5	**+2.0**		+5.5	V
V_{IL} (Logic "0")	0		**+0.8**	0		**+0.8**	V
I_{IH} (V_{IH} = 5.5V)		3	**10**		3	**10**	µA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error @ +25°C		±1/4	**±1/2**		±1/8	**±1/4**	LSB
$T_A = T_{min}$ to T_{max}		±1/2	**±3/4**		±1/4	**±1/2**	LSB
Differential Linearity Error @ +25°C		±1/2	**±3/4**		±1/4	**±1/2**	LSB
$T_A = T_{min}$ to T_{max}	**Monotonicity Guaranteed**			**Monotonicity Guaranteed**			LSB
Gain Error[2]		±0.1	**±0.2**		±0.1	**±0.2**	% of FSR[3]
Unipolar Offset Error[2]		±1	**±2**		±1	**±2**	LSB
Bipolar Zero[2]		±0.05	**±0.1**		±0.05	**±0.1**	% of FSR
DRIFT							
Differential Linearity		±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for							
FSR Change (2kΩ‖500pF load)							
with 10kΩ Feedback		3	4		3	4	µs
with 5kΩ Feedback		2	3		2	3	µs
For LSB Change		1			1		µs
Slew Rate	10			10			V/µs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			mA
Output Impedance (dc)		0.05			0.05		Ω
Short Circuit Current			40			40	mA
REFERENCE OUTPUT	**9.90**	10.00	**10.10**	**9.90**	10.00	**10.10**	V
External Current	0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5V dc		5	**10**		5	**10**	ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	**10**		5	**10**	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±12, ±15			±12, ±15		V
Range[4]	**±11.4**		**±16.5**	**±11.4**		**±16.5**	V
Supply Current							
+11.4 to +16.5V dc		8	12		8	12	mA
−11.4 to −16.5V dc		20	25		20	25	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	−65		+125	−65		+125	°C

NOTES

[1] The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.

[2] Adjustable to zero.

[3] FSR means "Full Scale Range" and is 20V for ±10V range and 10V for the ±5V range.

[4] A minimum power supply of ±12.5V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TIMING SPECIFICATIONS

(All Models, T_A = 25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V)

Symbol	Parameter	Min	Typ	Max	
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

ABSOLUTE MAXIMUM RATINGS

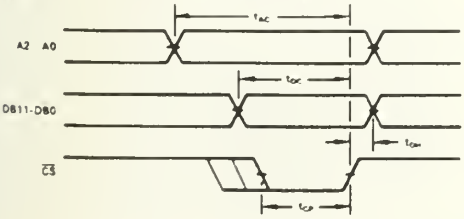
V_{CC} to Power Ground	0V to +18V
V_{EE} to Power Ground	0V to −18V
Digital Inputs (Pins 11–15, 17–28) to Power Ground	−1.0V to +7.0V
Ref In to Reference Ground	±12V
Bipolar Offset to Reference Ground	±12V
10V Span R to Reference Ground	±12V
20V Span R to Reference Ground	±24V
Ref Out, V_{OUT} (Pins 6, 9)	Indefinite short to power ground Momentary Short to V_{CC}
Power Dissipation	1000mW

Model	AD667A			AD667B			AD667S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
DIGITAL INPUTS										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible, $T_{min}-T_{max}$)[1]										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.7	V
I_{IH} (V_{IH} = 5.5V)		3	10		3	10		3	10	μA
I_{IL} (V_{IL} = 0.8V)		1	5		1	5		1	5	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4		±1/8	±1/2	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2		±1/4	±3/4	LSB
$T_A = T_{min}$ to T_{max}	Monotonicity Guaranteed			Monotonicity Guaranteed			Monotonicity Guaranteed			LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2		±0.1	±0.2	% of FSR[3]
Unipolar Offset Error[2]		±1	±2		±1	±2		±1	±2	LSB
Bipolar Zero[2]		±0.05	±0.1		±0.05	±0.1		±0.05	±0.1	% of FSR
DRIFT										
Differential Linearity		±2			±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} or T_{max}		±5	±30		±5	±15		±15	±30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} or T_{max}		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{min} or T_{max}		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
ANALOG OUTPUT										
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
REFERENCE OUTPUT	9.90	10.00	10.10	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY										
V_{CC} = +11.4 to +16.5V dc		5	10		5	10		5	10	ppm of FS/%
V_{EE} = −11.4 to −16.5V dc		5	10		5	10		5	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±12, ±15			±12, ±15			±12, ±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	±11.4		±16.5	V
Supply Current										
+11.4 to +16.5V dc		8	12		8	12		8	12	mA
−11.4 to −16.5V dc		20	25		20	25		20	25	mA
TEMPERATURE RANGE										
Specification	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C

TIMING DIAGRAMS

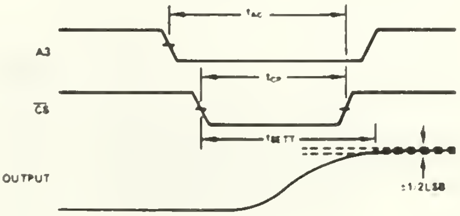
WRITE CYCLE #1

(Load First Rank from Data Bus; A3 = 1)

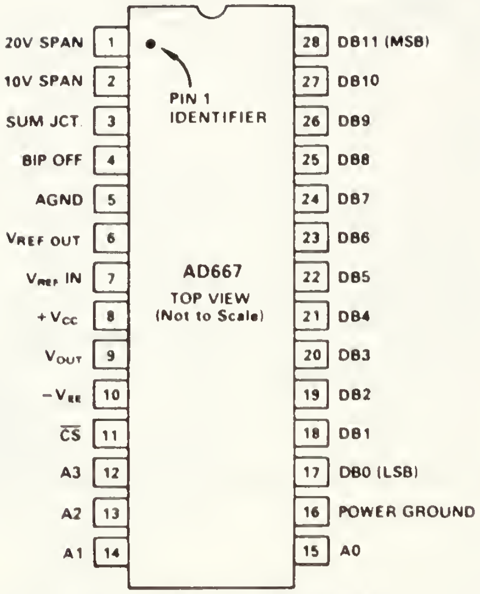


WRITE CYCLE #2

(Load Second Rank from First Rank; A2, A1, A0 = 1)

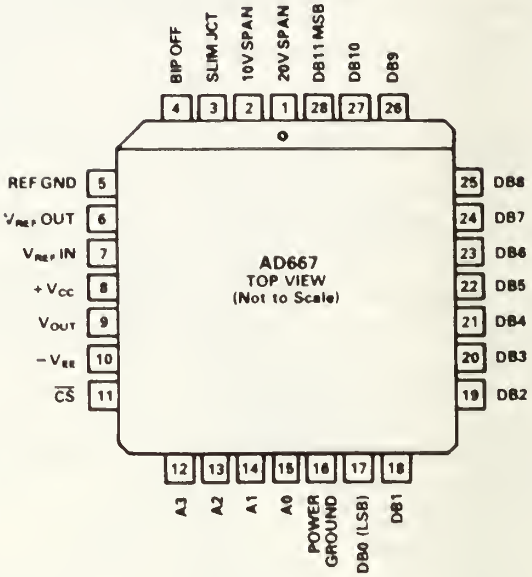


28-PIN DIP CONNECTIONS



*NOTE DIP PACKAGE PIN NUMBERS AND LCC CONTACT NUMBERS SERVE THE SAME FUNCTION.

PLCC, LCC PIN CONNECTIONS



ORDERING INFORMATION

Model	Package Options*	Temperature Range – °C	Linearity Error Max @ 25°C	Gain T.C. Max ppm/°C
AD667JN	Plastic DIP (N-28)	0 to +70	±1/2LSB	30
AD667JP	PLCC (P-28A)	0 to +70	±1/2LSB	30
AD667KN	Plastic DIP (N-28)	0 to +70	±1/4LSB	15
AD667KP	PLCC (P-28A)	0 to +70	±1/4LSB	15
AD667AD	Ceramic DIP (D-28)	−25 to +85	±1/2LSB	30
AD667AE	LCC (E-28A)	−25 to +85	±1/2LSB	30
AD667BD	Ceramic DIP (D-28)	−25 to +85	±1/4LSB	15
AD667BE	LCC (E-28A)	−25 to +85	±1/4LSB	15
AD667SD	Ceramic DIP (D-28)	−55 to +125	±1/2LSB	30
AD667SE	LCC (E-28A)	−55 to +125	±1/2LSB	30

*See Section 14 for package outline information.

THE AD667 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD667 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and B versions and 1/2LSB for the J, A and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD667 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be –1.83mV, or –3/4LSB. The AD667K and B grades have a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2 LSB.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD667 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V.

Gain and offset drift are minimized in the AD667 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table I.

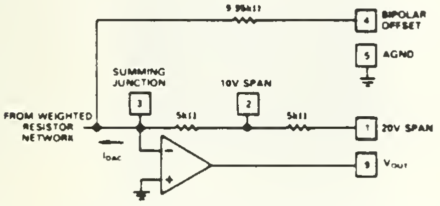


Figure 1. Output Amplifier Voltage Range Scaling Circuit

UNIPOLAR CONFIGURATION (Figure 2)

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar offset terminal, pin 4, should be grounded if not used for trimming.

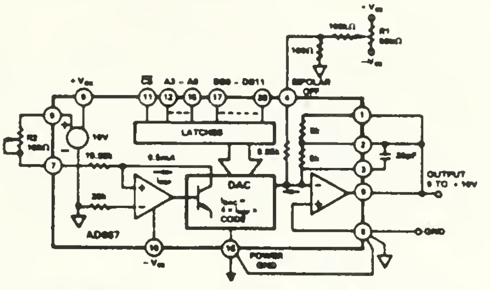


Figure 2. 0 to +10V Unipolar Voltage Output

STEP I . . . ZERO ADJUST
Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and pin 4 should be connected to pin 5.

STEP II . . . GAIN ADJUST
Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.)

BIPOLAR CONFIGURATION (Figure 3)

This configuration will provide a bipolar output voltage from –5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST
Turn OFF all bits. Adjust 100Ω trimmer R1 to give –5.000 volts output.

STEP II . . . GAIN ADJUST
Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

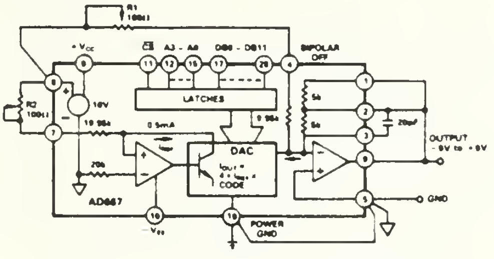


Figure 3. ±5V Bipolar Voltage Output

Output Range	Digital Input Codes	Connect Pin 9 to	Connect Pin 1 to	Connect Pin 2 to	Connect Pin 4 to
±10V	Offset Binary	1	9	NC	6 (through 50Ω fixed or 100Ω trim resistor)
±5V	Offset Binary	1 and 2	2 and 9	1 and 9	6 (through 50Ω fixed or 100Ω trim resistor)
±2.5V	Offset Binary	2	3	9	6 (through 50Ω fixed or 100Ω trim resistor)
0 to +10V	Straight Binary	1 and 2	2 and 9	1 and 9	5 (or optional trim – See Figure 2)
0 to +5V	Straight Binary	2	3	9	5 (or optional trim – See Figure 2)

Table I. Output Voltage Range Connections

INTERNAL/EXTERNAL REFERENCE USE

The AD667 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD667 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale error and bipolar offset) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset). A minimum of 0.1mA is available for driving external loads. The AD667 reference output should be buffered with an external op amp if it is required to supply more than 0.1mA output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

If an external reference is used (10.000V, for example), additional trim range must be provided, since the internal reference has a tolerance of ±1%, and the AD667 full-scale and bipolar offset are both trimmed with the internal reference. The gain and offset trim resistors give about ±0.25% adjustment range, which is sufficient for the AD667 when used with the internal reference.

It is also possible to use external references other than 10 volts. The recommended range of reference voltage is from +8 to +11 volts, which allows both 8.192V and 10.24V ranges to be used. The AD667 is optimized for fixed-reference applications. If the reference voltage is expected to vary over a wide range in a particular application, a CMOS multiplying DAC is a better choice.

Reduced values of reference voltage will also permit the ±12 volt ±5% power supply requirement to be relaxed to ±12 volts ±10%.

It is not recommended that the AD667 be used with external feedback resistors to modify the scale factor. The internal resistors are trimmed to ratio-match and temperature-track the other resistors on the chip, even though their absolute tolerances are ±20%, and absolute temperature coefficients are approximately −50ppm/°C. If external resistors are used, a wide trim range (±20%) will be needed and temperature drift will be increased to reflect the mismatch between the temperature coefficients of the internal and external resistors.

Small resistors may be added to the feedback resistors in order to accomplish small modifications in the scaling. For example, if a 10.24V full-scale is desired, a 140Ω 1% low-TC metal-film resistor can be added in series with the internal (nominal) 5k feedback resistor, and the gain trim potentiometer (between pins 6 and 7) should be increased to 200Ω. In the bipolar mode, increase the value of the bipolar offset trim potentiometer also to 200Ω.

GROUNDING RULES

The AD667 brings out separate analog and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths.

The analog ground at pin 5 is the ground point for the output amplifier and is thus the "high quality" ground for the AD667; it should be connected directly to the analog reference point of the system. The power ground at pin 16 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

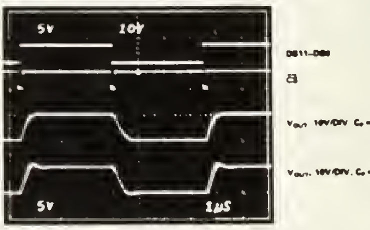
It is also important to apply decoupling capacitors properly on the power supplies for the AD667 and the output amplifier. The correct method for decoupling is to connect a capacitor from each power supply pin of the AD667 to the analog ground pin of the AD667. Any load driven by the output amplifier should also be referred to the analog ground pin.

OPTIMIZING SETTLING TIME

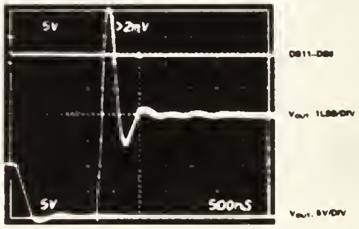
The dynamic performance of the AD667's output amplifier can be optimized by adding a small (20pF) capacitor across the feedback resistor. Figure 4 shows the improvement in both large-signal and small-signal settling for the 10V range. In Figure 4a, the top trace shows the data inputs (DB11–DB0 tied together), the second trace shows the CS pulse (A3–A0 tied low), and the lower two traces show the analog outputs for $C_F = 0$ and 20pF respectively.

Figures 4b and 4c show the settling time for the transition from all bits on to all bits off. Note that the settling time to ±1/2LSB for the 10V step is improved from 2.4 microseconds to 1.6 microseconds by the addition of the 20pF capacitor.

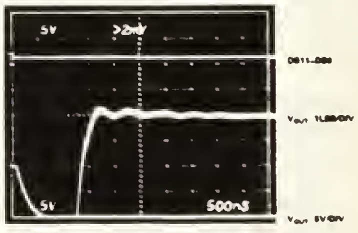
Figures 4d and 4e show the settling time for the transition from all bits off to all bits on. The improvement in settling time gained by adding $C_C = 20pF$ is similar.



a. Large Scale Settling

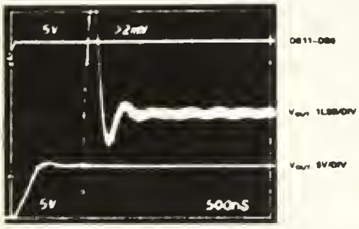


b. Fine-Scale Settling, $C_F = 0pF$

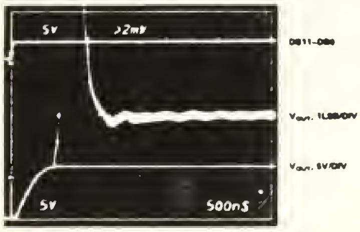


c. Fine-Scale Settling, $C_F = 20pF$

Figure 4. Settling Time Performance



d. Fine-Scale Settling, $C_F = 0pF$



e. Fine-Scale Settling, $C_F = 20pF$

Figure 4. Settling Time Performance (Continued)

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD667 consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers which can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 5 shows the block diagram of the AD667 logic section.

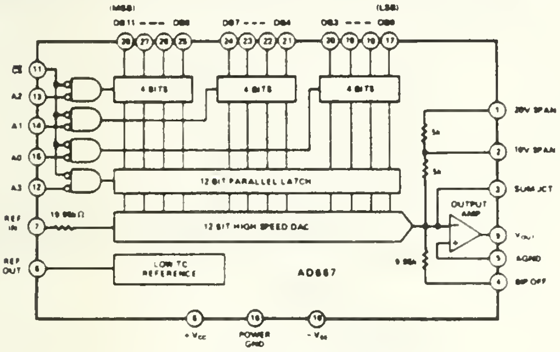


Figure 5. AD667 Block Diagram

The latches are controlled by the address inputs, A0-A3, and the $\overline{CS}$ input. All control inputs are active low, consistent with general practice in microprocessor systems. The four address lines each enable one of the four latches, as indicated in Table II.

All latches in the AD667 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. When any one of the control signals returns high, the data is latched.

It is permissible to enable more than one of the latches simultaneously. If a first rank latch is enabled coincident with the second rank latch, the data will reach the second rank correctly if the "WRITE CYCLE #1" timing specifications are met.

$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table II. AD667 Truth Table

INPUT CODING

The AD667 uses positive-true binary input coding. Logic "1" is represented by an input voltage greater than 2.0V and logic "0" is defined as an input voltage less than 0.8V.

Unipolar coding is straight binary, where all zeroes (000_H) on the data inputs yields a zero analog output and all ones (FFF_H) yields an analog output 1LSB below full scale.

Bipolar coding is offset binary, where an input code of 000_H yields a minus full-scale output, an input of FFF_H yields an output 1LSB below positive full scale, and zero occurs for an input code with only the MSB on (800_H).

The AD667 can be used with two's complement input coding if an inverter is used on the MSB (DB11).

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can thus interface with any type of 5 volt logic. The configuration of the input circuit is shown in Figure 6.

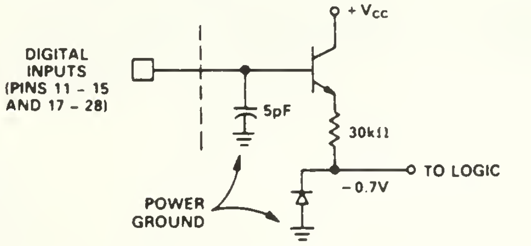


Figure 6. Equivalent Digital Input Circuit

The AD667 data and control inputs will float to a logic 0 if left open. It is recommended that any unused inputs be connected to power ground to improve noise immunity.

Fanout for the AD667 is 100 when used with a standard low power Schottky gate output device.

8-BIT MICROPROCESSOR INTERFACE

The AD667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats.

Whenever a 12-bit DAC is loaded from an 8-bit bus, two bytes are required. If the program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the 4 most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4

DB3	DB2	DB1	DB0	X	X	X	X

a. Left Justified

X	X	X	X	DB11	DB10	DB9	DB8

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

b. Right Justified

Figure 7. 12-Bit Data Formats for 8-Bit Systems

Figure 8 shows an addressing scheme for use with an AD667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the AD667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

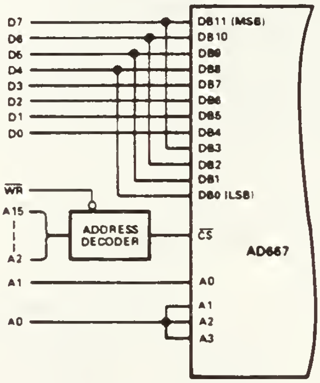


Figure 8. Left-Justified 8-Bit Bus Interface

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD667 still occupies two adjacent locations in the processor's memory map. In the circuit of Figure 9, location X01 loads the 8LSBs and location X10 loads the 4MSBs and updates the output.

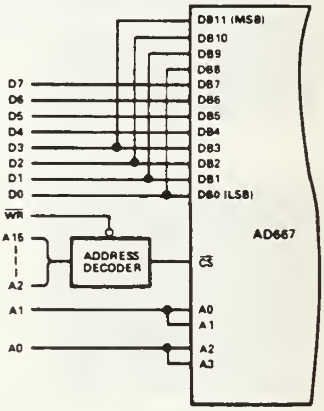


Figure 9. Right-Justified 8-Bit Bus Interface

USING THE AD667 WITH 12- AND 16-BIT BUSES

The AD667 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines (A0 through A3) are tied low, and the latch is enabled by $\overline{CS}$ going low. The AD667 thus occupies a single memory location.

This configuration uses the first and second rank registers simultaneously. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is low will cause activity at the AD667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

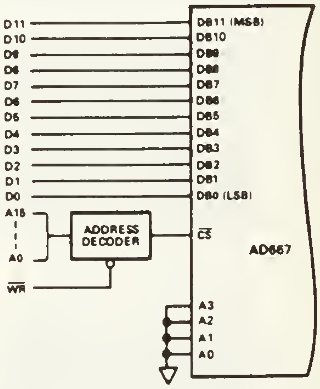


Figure 10. Connections for 12- and 16-Bit Bus Interface

APPENDIX F

FIFO MEMORY TECHNICAL DATA (IDT 7201 SA 120DB)

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 256 x 9-BIT & 512 x 9-BIT

IDT7200S/L
IDT7201SA/LA

FEATURES:

- First-In/First-Out dual-port memory
- 256 x 9 organization (IDT7200)
- 512 x 9 organization (IDT7201A)
- Low power consumption
  - Active: 770mW (max.)
  - Power-down: 27.5mW (max.)
- Ultra high speed—15ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with 720X family
- Status Flags: Empty, Half-Full, Full
- Auto-retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-87531, 5962-89666, and 5962-89863 are listed on this function.

DESCRIPTION:

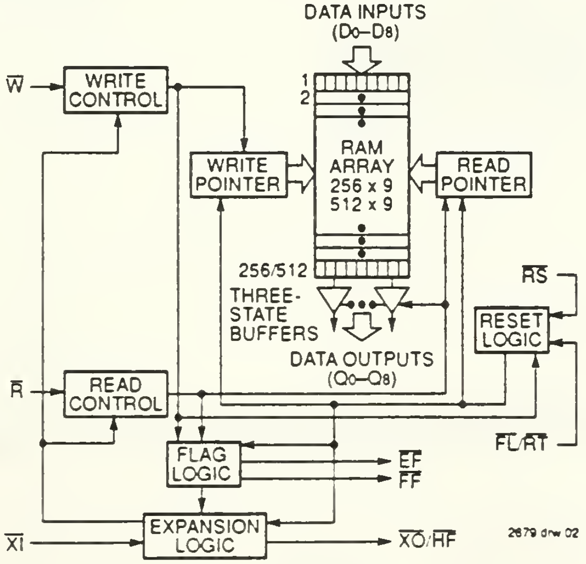
The IDT7200/7201A are dual-port memories that load and empty data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a read/write cycle time of 25ns (40MHz).

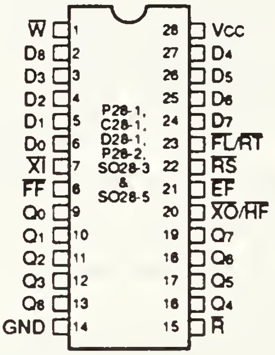
The devices utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7200/1A is fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

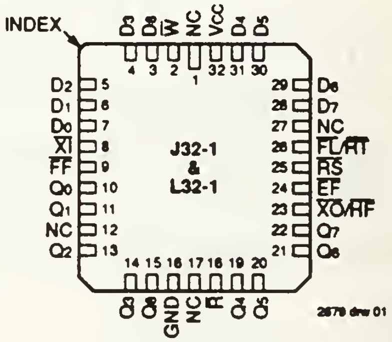
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/FLATPACK
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2679 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2679 tbl 02

1. This parameter is sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}[1]	Input High Voltage Commercial	2.0	—	—	V
V_{IH}[1]	Input High Voltage Military	2.2	—	—	V
V_{IL}[2]	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2679 tbl 03

1. V_{IH} = 2.6V for $\overline{XI}$ input (commercial).
   V_{IH} = 2.8V for $\overline{XI}$ input (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT7200 IDT7201 Commercial t_A = 15,20ns			IDT7200 IDT7201 Military t_A = 20ns			IDT7200 IDT7201 Commercial t_A = 25,35ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	–1	—	1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OH} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	140(4)	—	—	160(4)	—	—	125(4)	mA
I_{CC2}(3)	Standby Current ($\overline{R}=\overline{W}=\overline{RS}=\overline{FL}/\overline{RT}=V_{IH}$)	—	—	15	—	—	20	—	—	15	mA
I_{CC3}(L)(3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	5	—	—	9	—	—	0.5	mA
I_{CC3}(S)(3)	Power Down Current (All Input = V_{CC} - 0.2V)							—	—	5	mA

2679 tbl 04

DC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT7200 IDT7201 Military t_A = 30,40ns			IDT7200 IDT7201 Commercial t_A = 50,65,80,120ns			IDT7200 IDT7201 Military t_A = 50,65,80,120ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (Any Input)	–10	—	10	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OH} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	140(4)	—	50	80	—	70	100	mA
I_{CC2}(3)	Standby Current ($\overline{R}=\overline{W}=\overline{RS}=\overline{FL}/\overline{RT}=V_{IH}$)	—	—	20	—	5	8	—	8	15	mA
I_{CC3}(L)(3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	0.9	—	—	0.5	—	—	0.9	mA
I_{CC3}(S)(3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	9	—	—	5	—	—	9	mA

2679 tbl 05

NOTES:

1 Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2 $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3 I_{CC} measurements are made with outputs open (only capacitive loading).
4 Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5.0V \pm 10\%$, $T_A = 0°C$ to $+70°C$; Military: $V_{CC} = 5.0V \pm 10\%$, $T_A = -55°C$ to $+125°C$)

		Com'l.		Com'l. & Mil.		Com'l.		Mil.		Com'l.		
		7200L15 7201LA15		7200L20 7201LA20		7200S/L25 7201SA/LA25		7200S/L30 7201SA/LA30		7200S/L35 7201SA/LA35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	40	—	33.3	—	28.5	—	25	—	22.2	MHz
t_{RC}	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	5	—	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	15	—	15	—	18	—	20	—	20	ns
t_{WC}	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{WPW}	Write Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	11	—	12	—	15	—	18	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RS}	Reset Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RSS}	Reset Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
t_{RT}	Retransmit Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{RTS}	Retransmit Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	25	—	30	—	35	—	40	—	45	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	25	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	15	—	20	—	25	—	30	—	30	ns
t_{RFF}	Read High to Full Flag High	—	15	—	20	—	25	—	30	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	15	—	20	—	25	—	30	—	35	—	ns
t_{WEF}	Write High to Empty Flag High	—	15	—	20	—	25	—	30	—	30	ns
t_{WFF}	Write Low to Full Flag Low	—	15	—	20	—	25	—	30	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	25	—	30	—	35	—	40	—	45	ns
t_{RHF}	Read High to Half-Full Flag High	—	25	—	30	—	35	—	40	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	15	—	20	—	25	—	30	—	35	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	15	—	20	—	25	—	30	—	35	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	15	—	20	—	25	—	30	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	10	—	10	—	10	—	10	—	ns

2679 tbl 06

NOTES:

1. Timings referenced as in AC Test Conditions
2. Pulse widths less than minimum value are not allowed
3. Values guaranteed by design, not currently tested
4. Only applies to read data flow-through mode

AC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: Vcc = 5.0V±10%, TA = 0°C to +70°C; Military: Vcc = 5.0V±10%, TA = –55°C to +125°C)

		Military		Commmercial and Military								
		7200S/L40 7201SA/LA40		7200S/L50 7201SA/LA50		7200S/L65 7201SA/LA65		7200S/L80 7201SA/LA80		7200S/L120 7201SA/LA120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	20	—	15	—	12.5	—	10	—	7	MHz
t_{RC}	Read Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSS}	Reset Set-up Time[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTS}	Retransmit Set-up Time[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	80	—	100	—	140	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	35	—	45	—	60	—	60	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{WEF}	Write High to Empty Flag High	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	35	—	45	—	60	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	50	—	65	—	80	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	50	—	65	—	80	—	100	—	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	40	—	50	—	65	—	80	—	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	40	—	50	—	65	—	80	—	120	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	40	—	50	—	65	—	80	—	120	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	15	—	15	—	15	—	15	—	ns

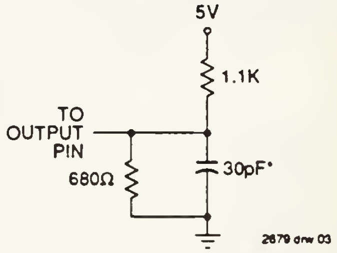
2679 tbl 08

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2679 tbl 08



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN ($D_0 - D_8$)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs ($Q_0 - Q_8$) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the restransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 256/512 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go low after 256 writes for IDT7200 and 512 writes for the IDT7201A.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0 – Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.

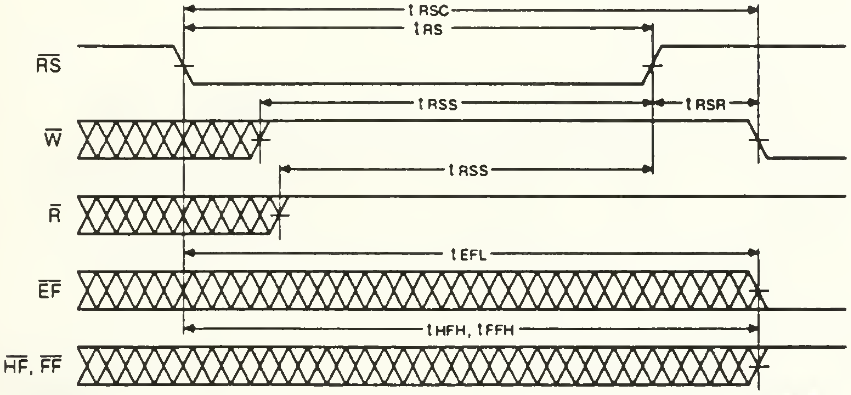


Figure 2. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

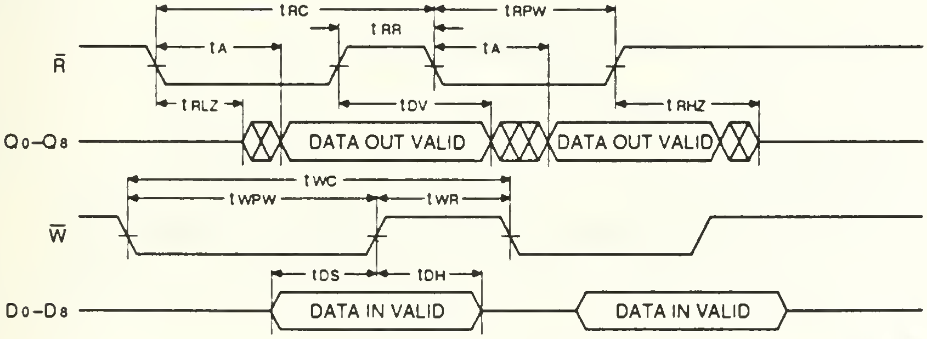
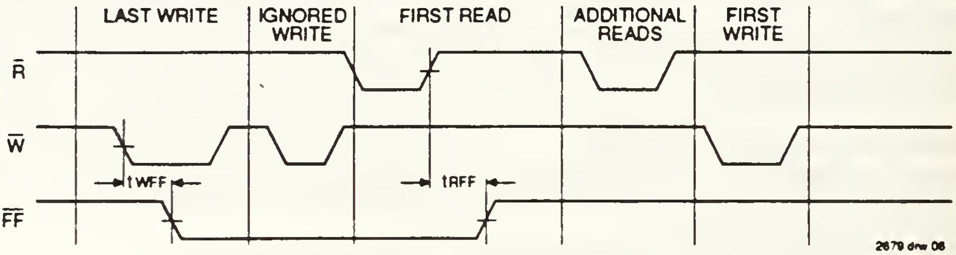
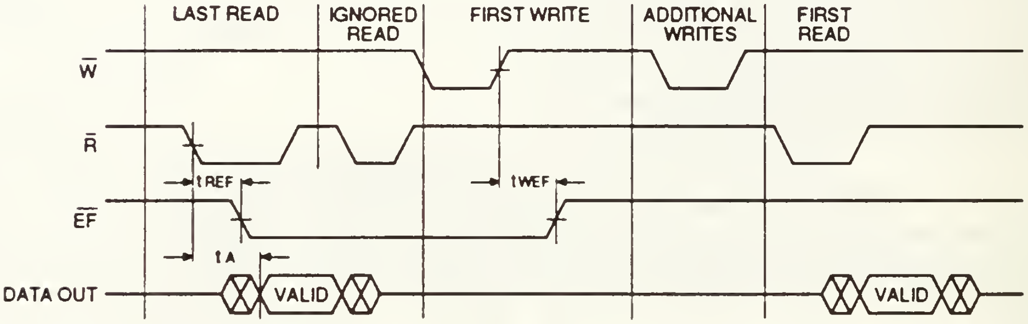


Figure 3. Asynchronous Write and Read Operation



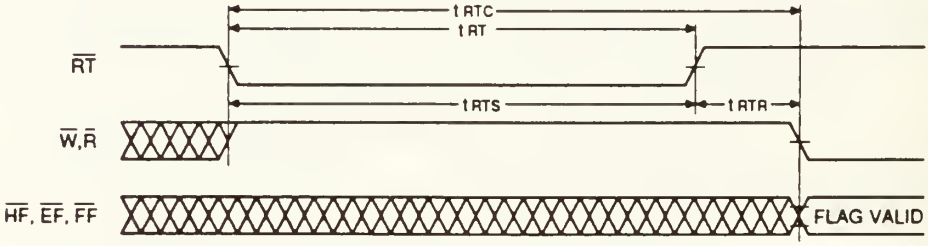
2679 drw 06

Figure 4. Full Flag From Last Write to First Read



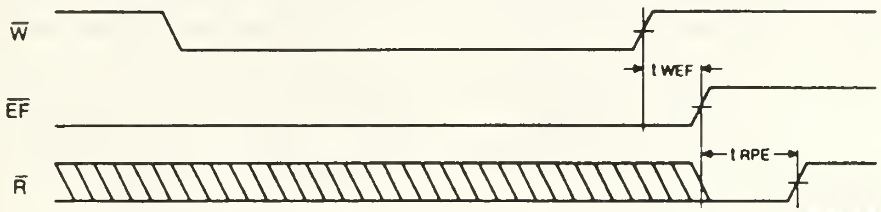
2679 drw 07

Figure 5. Empty Flag From Last Read to First Write



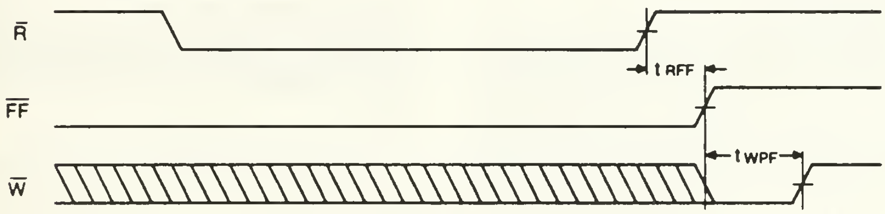
2679 drw 08

Figure 6. Retransmit



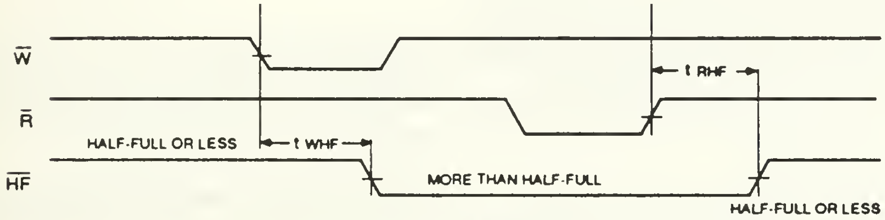
2679 drw 09

Figure 7. Empty Flag Timing



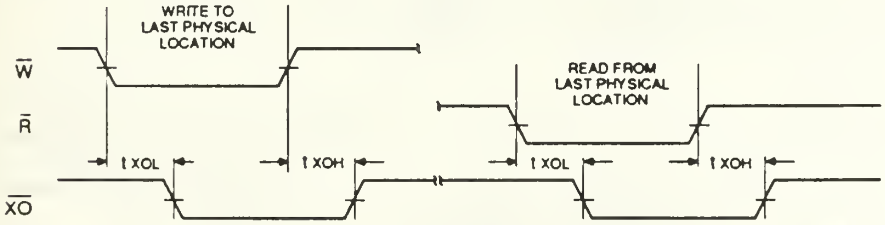
2679 drw 10

Figure 8. Full Flag Timing



2679 drw 11

Figure 9. Half-Full Flag Timing



2679 drw 12

Figure 10. Expansion Out

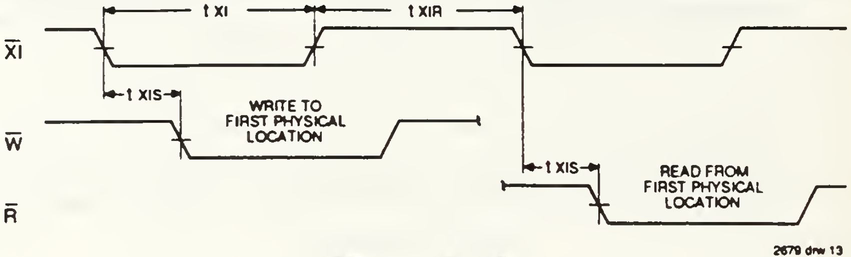


Figure 11. Expansion In

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7200/7201A may be used when the application requirements for 256/512 words or less. The IDT7200/7201A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12). In the mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

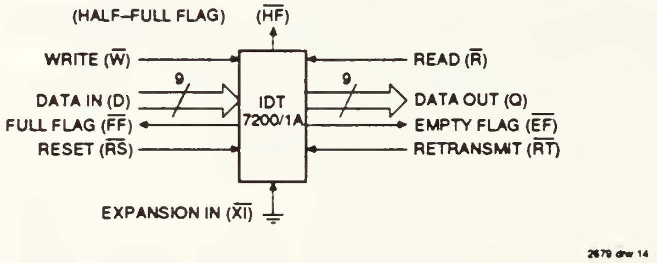


Figure 12. Block Diagram of Single 256/512 x 9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7201As. Any word width can be attained by adding additional IDT7201As.

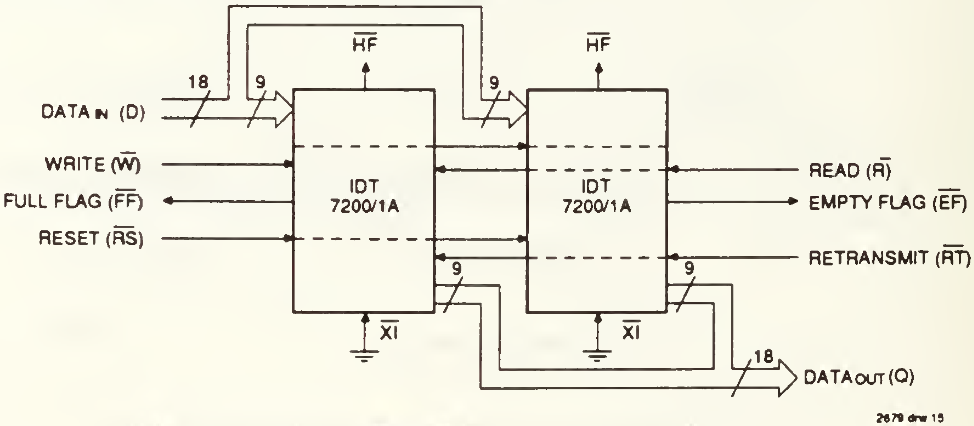


Figure 13. Block Diagram of 256/512 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DASIY CHAIN) MODE

The IDT7200/7201A can easily be adapted to applications where the requirements are for greater than 256/512 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201As. Any depth can be attained by adding additional IDT7200/7201As. The IDT7200/7201A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{\text{FL}}$) control input.
2. All other devices must have $\overline{\text{FL}}$ in the high state.
3. The Expansion Out ($\overline{\text{XO}}$) pin of each device must be tied to the Expansion In ($\overline{\text{XI}}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{\text{FF}}$) and Empty Flag ($\overline{\text{EF}}$). This requires the ORing of all $\overline{\text{EF}}$s and ORing of all $\overline{\text{FF}}$s (i.e. all must be set to generate the correct composite $\overline{\text{FF}}$ or $\overline{\text{EF}}$). See Figure 14.
5. The Retransmit ($\overline{\text{RT}}$) function and Half-Full Flag ($\overline{\text{HF}}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201As as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{\text{FF}}$ is monitored on the device where $\overline{\text{W}}$ is used; $\overline{\text{EF}}$ is monitored on the device where $\overline{\text{R}}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{\text{W}}$, called the first write edge, and it remains on the bus until the $\overline{\text{R}}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{\text{EF}}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{\text{R}}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will be de-assert the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{\text{R}}$ was low. On toggling $\overline{\text{R}}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{\text{R}}$ line causes the $\overline{\text{FF}}$ to be de-asserted but the $\overline{\text{W}}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{\text{W}}$, the new word is loaded in the FIFO. The $\overline{\text{W}}$ line must be toggled when $\overline{\text{FF}}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{\text{RS}}$	$\overline{\text{RT}}$	$\overline{\text{XI}}$	Read Pointer	Write Pointer	$\overline{\text{EF}}$	$\overline{\text{FF}}$	$\overline{\text{HF}}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:

2679 tbl 09

1. Pointer will increment if flag is High.

TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{\text{RS}}$	$\overline{\text{FL}}$	$\overline{\text{XI}}$	Read Pointer	Write Pointer	$\overline{\text{EF}}$	$\overline{\text{FF}}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:

2679 tbl 10

1. $\overline{\text{XI}}$ is connected to $\overline{\text{XO}}$ of previous device. See Figure 15. $\overline{\text{RS}}$ = Reset Input $\overline{\text{FL}}/\overline{\text{RT}}$ = First Load/Retransmit, $\overline{\text{EF}}$ = Empty Flag Output, $\overline{\text{FF}}$ = Flag Full Output, $\overline{\text{XI}}$ = Expansion Input, $\overline{\text{HF}}$ = Half-Full Flag Output

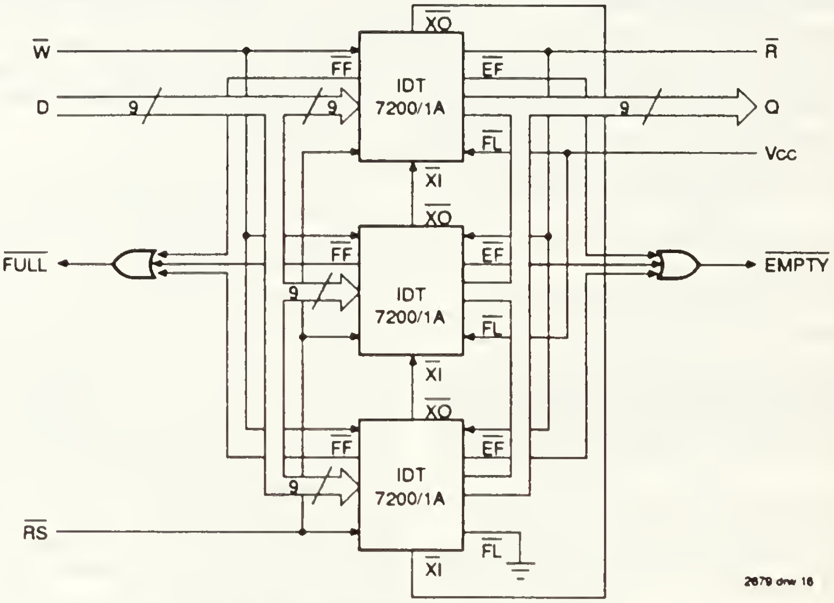


Figure 14. Block Diagram of 1538 x 9 FIFO Memory (Depth Expansion)

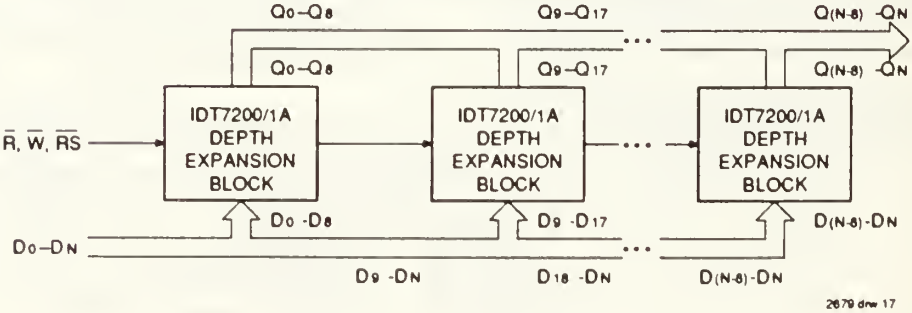


Figure 15. Compound FIFO Expansion

NOTES:
1 For depth expsansion block see section on Depth Expansion and Figure 14
2 For Flag detection see section on Width Expansion and Figure 13

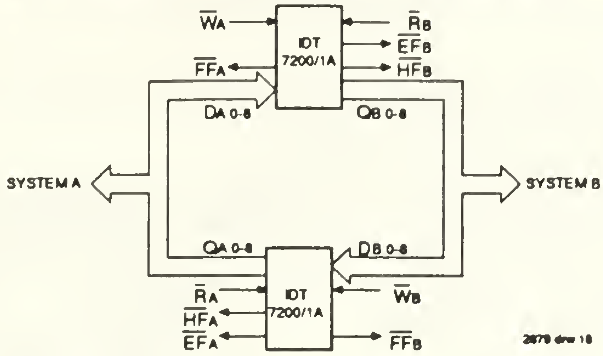


Figure 16. Bidirectional FIFO Mode

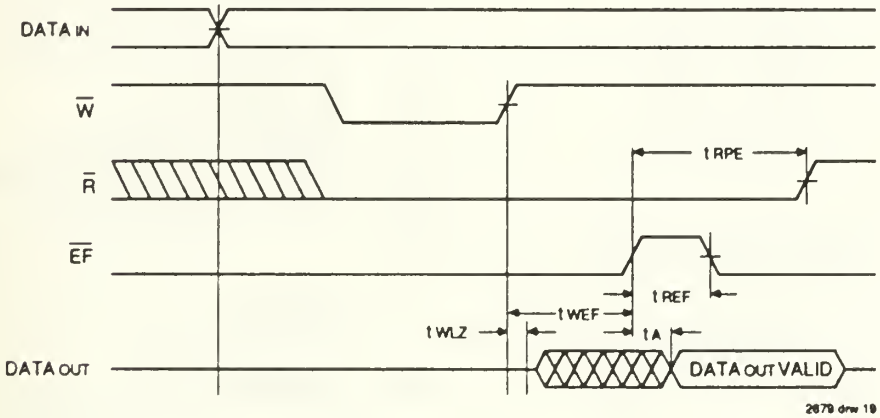


Figure 17. Read Data Flow-Through Mode

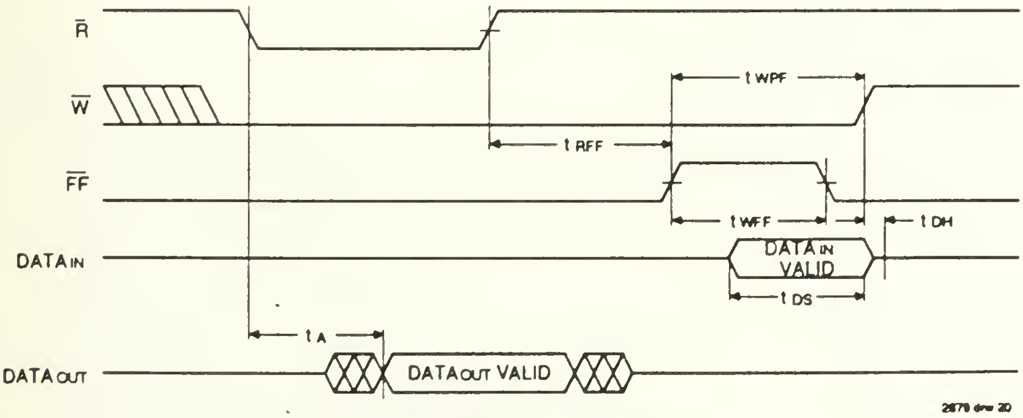


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT	XXXX	X	XXX	X	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Blank	Commercial (0°C to + 70°C)
B	Military (–55°C to + 125°C) Compliant to MIL-STD-883, Class B

P	Plastic DIP
TP	Plastic THINDIP
D	CERDIP
TC	Sidebraze THINDIP
J	Plastic Leaded Chip Carrier
SO	SOIC
Y	SOJ
L	Leadless Chip Carrier
XE	CERPACK

15	Commercial Only	Access Time (t_A) Speed in Nanoseconds
20		
25	Commercial Only	
30	Military Only	
35	Commercial Only	
40	Military Only	
50		
65		
80		
120		

SA	Standard Power*
LA	Low Power*

7200	256 x 9-Bit FIFO
7201	512 x 9-Bit FIFO

2679 drw 21

* "A" to be included for 7201 ordering part number only

APPENDIX G

OCTAL LATCH TECHNICAL DATA (SNJ54LS373)

SN54LS373, SN54LS374, SN54S373, SN54S374,
SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS
OCTOBER 1975—REVISED MARCH 1988

- **Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package**
- **3-State Bus-Driving Outputs**
- **Full Parallel-Access for Loading**
- **Buffered Control Inputs**
- **Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)**
- **P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)**

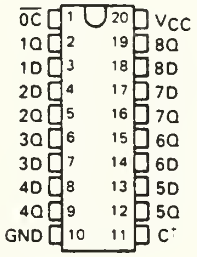
'LS373, 'S373
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

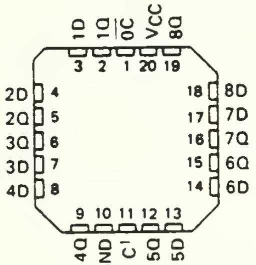
'LS374, 'S374
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . J OR W PACKAGE
SN74LS373, SN74LS374, SN74S373,
SN74S374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS373, SN54LS374, SN54S373,
SN54S374 . . . FK PACKAGE
(TOP VIEW)



*C for 'LS373 and 'S373 CLK for 'LS374 and S374

description

These 8-bit registers feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

description (continued)

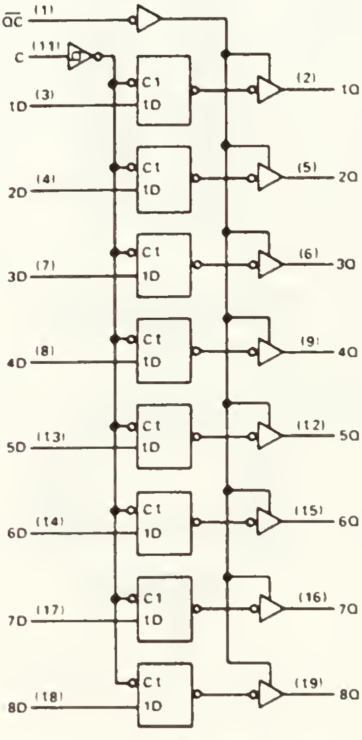
The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices, simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

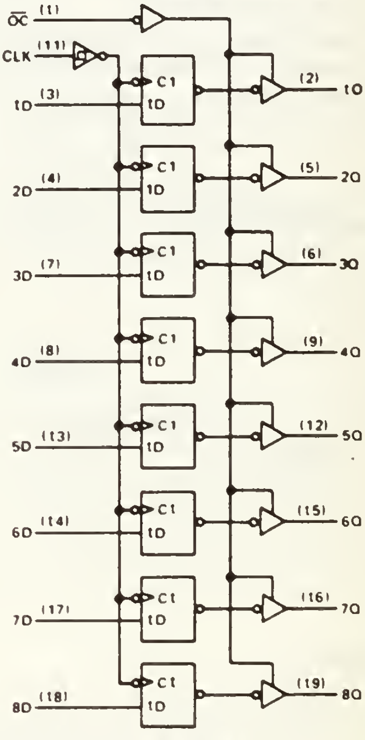
logic diagrams (positive logic)

'LS373, 'S373
TRANSPARENT LATCHES



⎍ for 'S373 only

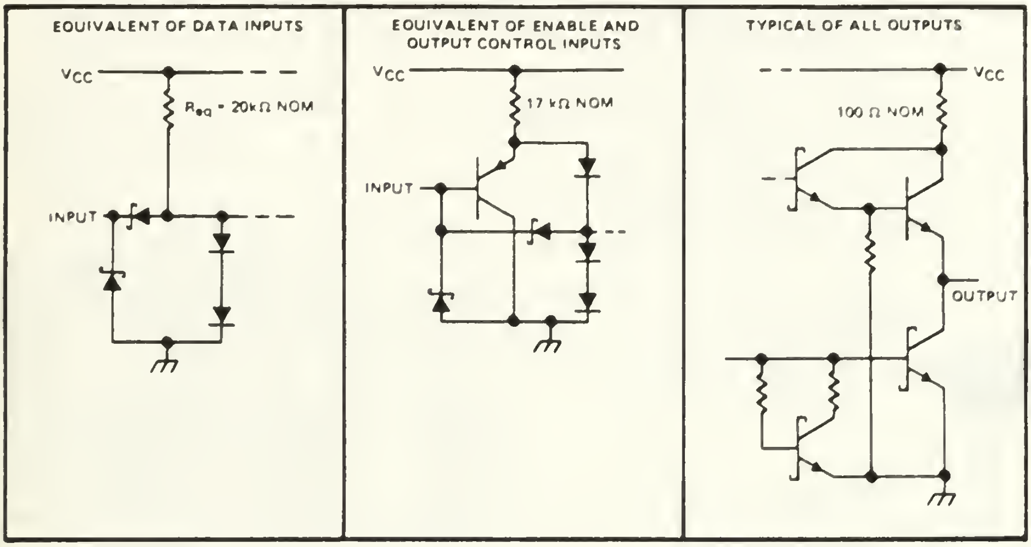
'LS374, 'S374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS



⎍ for 'S374 only

Pin numbers shown are for DW, J, N, and W packages schematic of inputs and outputs

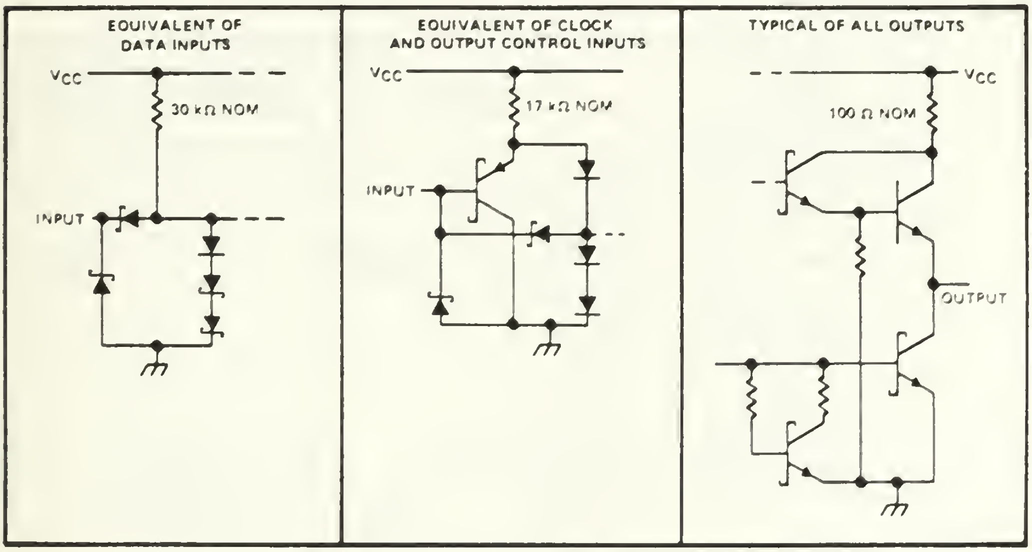
'LS373


EQUIVALENT OF DATA INPUTS

EQUIVALENT OF ENABLE AND OUTPUT CONTROL INPUTS

TYPICAL OF ALL OUTPUTS

'LS374


EQUIVALENT OF DATA INPUTS

EQUIVALENT OF CLOCK AND OUTPUT CONTROL INPUTS

TYPICAL OF ALL OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		7 V
Off-state output voltage		5.5 V
Operating free-air temperature range	SN54LS'	−55°C to 125°C
	SN74LS'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1 Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CLK high	15			15			ns
		CLK low	15			15			
t_{su}	Data setup time	'LS373	5↓			5↓			ns
		'LS374	20↑			20↑			
t_h	Data hold time	'LS373	20↓			20↓			ns
		'LS374[†]	5↑			0↑			
T_A	Operating free-air temperature		−55		125	0		70	°C

[†] The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns. (Commercial only)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS'			SN74LS'			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = -18$ mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, $V_{IH} = 2$ V, $V_{IL} = V_{IL}$max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, $V_{IH} = 2$ V, $V_{IL} = V_{IL}$max	$I_{OL} = 12$ mA		0.25	0.4		0.25	0.4	V
			$I_{OL} = 24$ mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, $V_{IH} = 2$ V, $V_O = 2.7$ V				20			20	µA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, $V_{IH} = 2$ V, $V_O = 0.4$ V				−20			−20	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX, $V_I = 7$ V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, $V_I = 2.7$ V				20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, $V_I = 0.4$ V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current[§]	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V	'LS373		24	40		24	40	mA
			'LS374		27	40		27	40	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25$ C.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

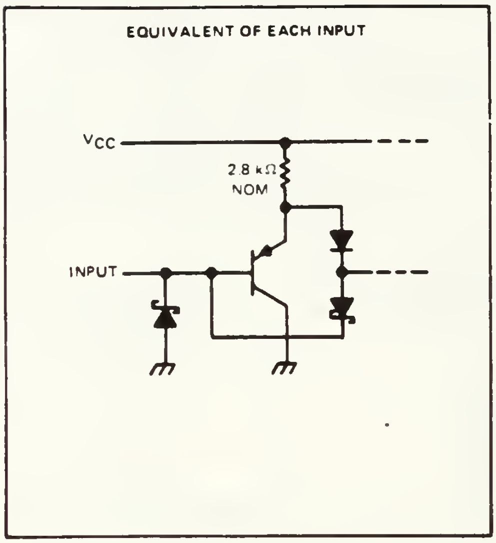
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS373			'LS374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			$C_L = 45$ pF, $R_L = 667\ \Omega$ See Notes 2 and 3				35	50		MHz
t_{PLH}	Data	Any Q			12	18				ns
t_{PHL}					12	18				
t_{PLH}	Clock or enable	Any Q			20	30		15	28	ns
t_{PHL}					18	30		19	28	
t_{PZH}	Output Control	Any Q			15	28		20	26	ns
t_{PZL}					25	36		21	28	
t_{PHZ}	Output Control	Any Q	$C_L = 5$ pF, $R_L = 667\ \Omega$ See Note 3		15	25		15	28	ns
t_{PLZ}	Output Control	Any Q			12	20		12	20	ns

NOTES 2 Maximum clock frequency is tested with all outputs loaded
3 Load circuits and voltage waveforms are shown in Section 1

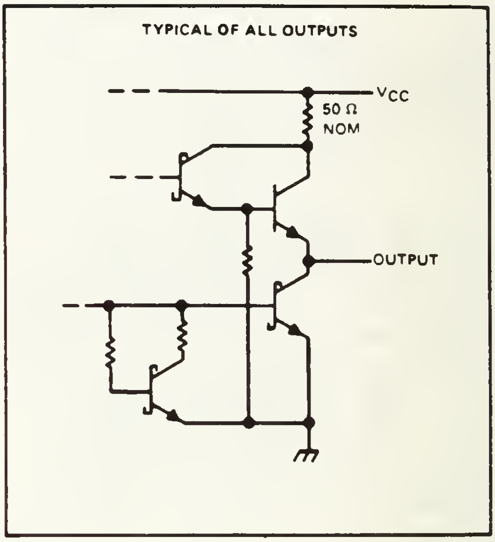
f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

schematic of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54S'	−55°C to 125°C
	SN74S'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1 Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−2			−6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{su}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_h	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]			MIN	TYP[‡]	MAX	UNIT
V_{IH}					2			V
V_{IL}							0.8	V
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	SN54S'	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX			2.4	3.4		V
	SN74S'				2.4	3.1		
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5	V
I_{OZH}		V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V					50	μA
I_{OZL}		V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V					−50	μA
I_I		V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V					50	μA
I_{IL}		V_{CC} = MAX, V_I = 0.5 V					−250	μA
I_{OS}[§]		V_{CC} = MAX			−40		−100	mA
I_{CC}		V_{CC} = MAX	'S373	outputs high			160	mA
				outputs low			160	
				outputs disabled			190	
			'S374	outputs high			110	
				outputs low			140	
				outputs disabled			160	
				CLK and $\overline{OC}$ at 4 V, D inputs at 0 V			180	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

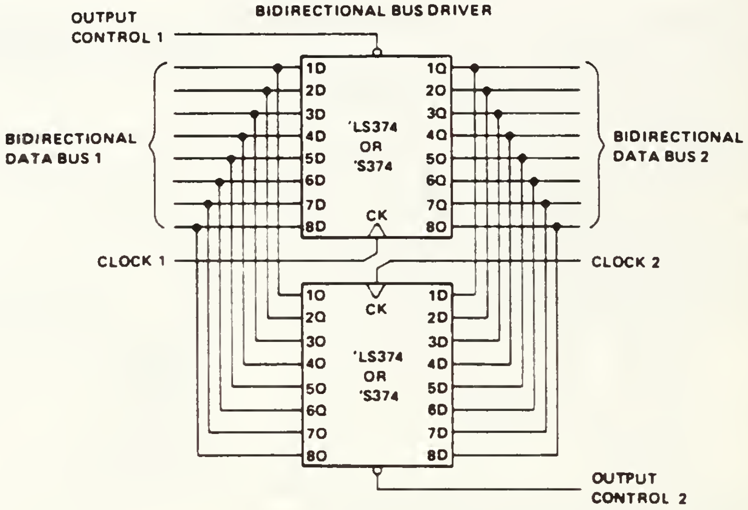
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Notes 2 and 4				75	100		MHz
t_{PLH}	Data	Any Q			7	12				ns
t_{PHL}					7	12				
t_{PLH}	Clock or enable	Any Q			7	14		8	15	ns
t_{PHL}					12	18		11	17	
t_{PZH}	Output Control	Any Q			8	15		8	15	ns
t_{PZL}					11	18		11	18	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 280 Ω, See Note 3		6	9		5	9	ns
t_{PLZ}					8	12		7	12	

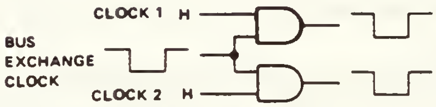
NOTES 2 Maximum clock frequency is tested with all outputs loaded
4 Load circuits and voltage waveforms are shown in Section 1

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

TYPICAL APPLICATION DATA

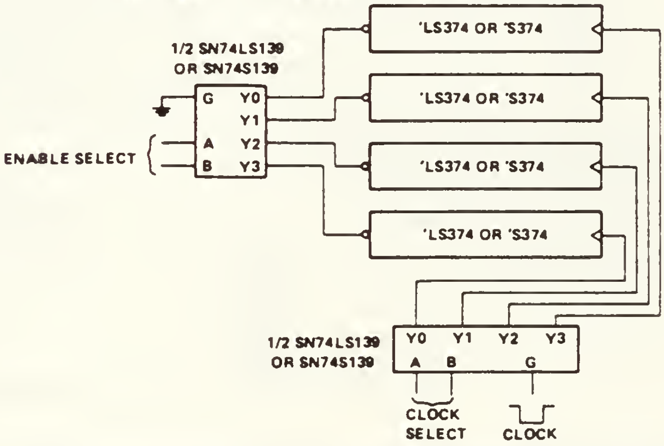
BIDIRECTIONAL BUS DRIVER





CLOCK CIRCUIT FOR BUS EXCHANGE

EXPANDABLE 4-WORD-BY-8-BIT GENERAL REGISTER FILE



APPENDIX H

OCTAL BUFFER TECHNICAL DATA (SNJ54LS244)

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

APRIL 1985 – REVISED MARCH 1988

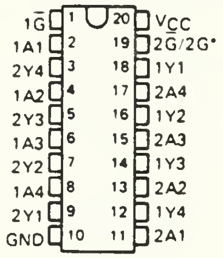
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **PNP Inputs Reduce D-C Loading**
- **Hysteresis at Inputs Improves Noise Margins**

description

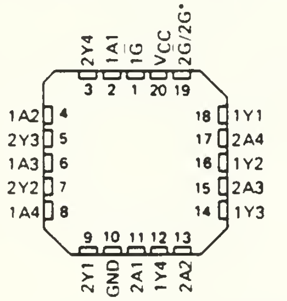
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54LS', SN54S' . . . J OR W PACKAGE
SN74LS', SN74S' . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS', SN54S' . . . FK PACKAGE
(TOP VIEW)

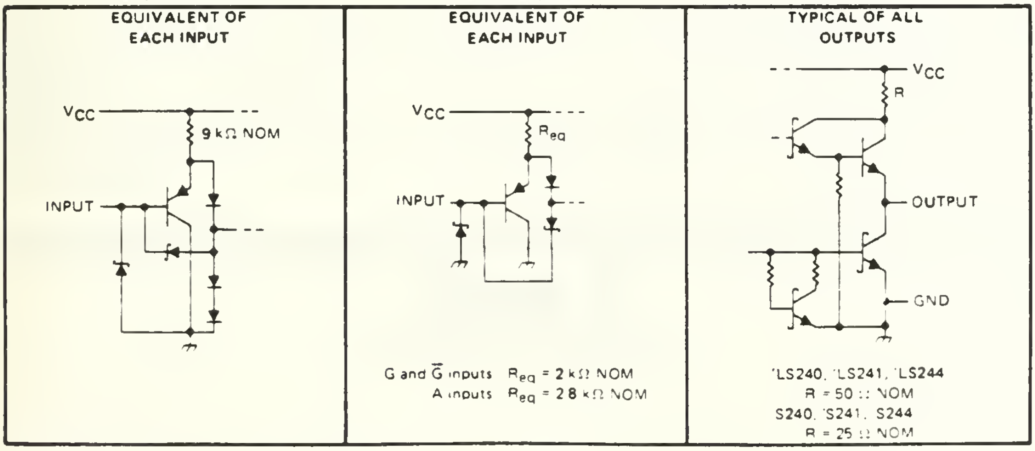


*2G for 'LS241 and 'S241 or $\overline{2G}$ for all other drivers

schematics of inputs and outputs

'LS240, 'LS241, 'LS244

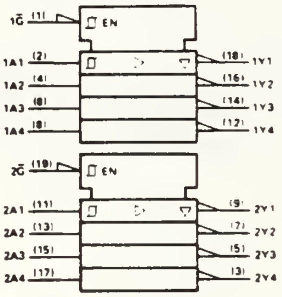
'S240, 'S241, 'S244



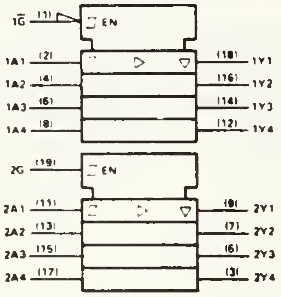
SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244, SN74SL240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

logic symbols†

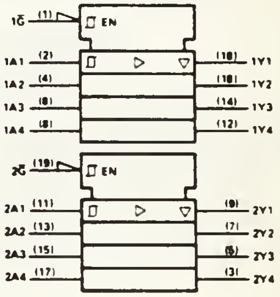
'LS240, 'S240



'LS241, 'S241



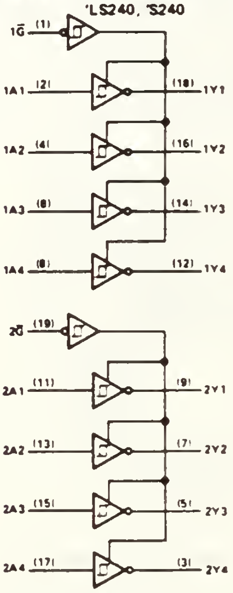
'LS244, 'S244



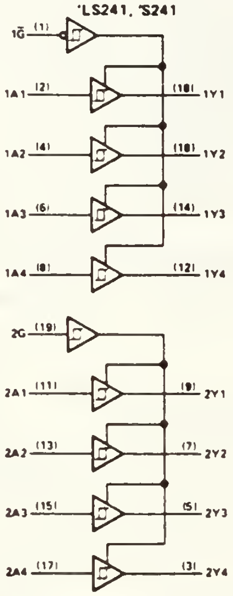
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

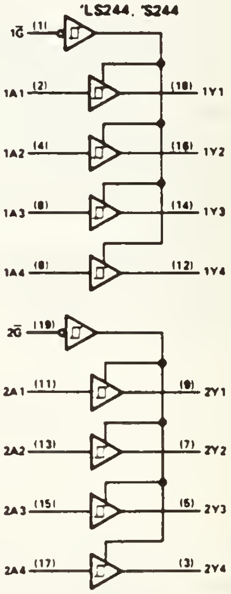
'LS240, 'S240



'LS241, 'S241



'LS244, 'S244



Pin numbers shown are for DW, J, N, and W packages

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS Circuits	7 V
'S Circuits	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS', SN54S' Circuits	−55°C to 125°C
SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			− 12			− 15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	− 55		125	0		70	°C

NOTE 1 Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		SN54LS'			SN74LS'			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN I_I = − 18 mA				− 1.5			− 1.5	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = − 3 mA		2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX		2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA			0.4			0.4	V
			I_{OL} = 24 mA						0.5	
I_{OZH}		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX	V_O = 2.7 V			20			20	μA
I_{OZL}			V_O = 0.4 V			− 20			− 20	
I_I		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}		V_{CC} = MAX, V_{IL} = 0.4 V				− 0.2			− 0.2	mA
I_{OS}[§]		V_{CC} = MAX		− 40		− 225	− 40		− 225	mA
I_{CC}	Outputs high	V_{CC} = MAX, Output open	All		17	27		17	27	mA
	Outputs low		'LS240		26	44		26	44	
			'LS241, 'LS244		27	46		27	46	
	All outputs disabled		'LS240		29	50		29	50	
			'LS241, 'LS244		32	54		32	54	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	R_L = 667 Ω, See Note 2	C_L = 45 pF,		9	14		12	18	ns
t_{PHL}				12	18		12	18	ns
t_{PZL}				20	30		20	30	ns
t_{PZH}				15	23		15	23	ns
t_{PLZ}	R_L = 667 Ω, See Note 2	C_L = 5 pF.		10	20		10	20	ns
t_{PHZ}				15	25		15	25	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1

SN54S240, SN54S241, SN54S244, SN74S240, SN74S241, SN74S244, OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER		SN54S' MIN	SN54S' NOM	SN54S' MAX	SN74S' MIN	SN74S' NOM	SN74S' MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			– 12			– 15	mA
I_{OL}	Low-level output current			48			64	mA
	External resistance between any input and V_{CC} or ground			40			40	kΩ
T_A	Operating free-air temperature (see Note 3)	– 55		125	0		70	°C

NOTES 1 Voltage values are with respect to network ground terminal.

3 An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S' MIN	SN54S' TYP‡	SN54S' MAX	SN74S' MIN	SN74S' TYP‡	SN74S' MAX	UNIT
V_{IK}		V_{CC} = MIN, I_I = – 18 mA				– 1.2			– 1.2	V
Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = – 1 mA					2.7			V
		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = – 3 mA		2.4	3.4		2.4	3.4		
		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX		2			2			
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.55			0.55	V
I_{OZH}		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50	μA
I_{OZL}			V_O = 0.5 V			– 50			– 50	
I_I		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Any A	V_{CC} = MAX, V_I = 0.5 V				– 400			– 400	μA
	Any G					– 2			– 2	mA
I_{OS}§		V_{CC} = MAX		– 50		– 225	– 50		– 225	mA
I_{CC}	Outputs high	V_{CC} = MAX, Outputs open	'S240		80	123		80	135	mA
			'S241, 'S244		95	147		95	160	
	Outputs low		'S240		100	145		100	150	
			'S241, 'S244		120	170		120	180	
	Outputs disabled		'S240		100	145		100	150	
			'S241, 'S244		120	170		120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

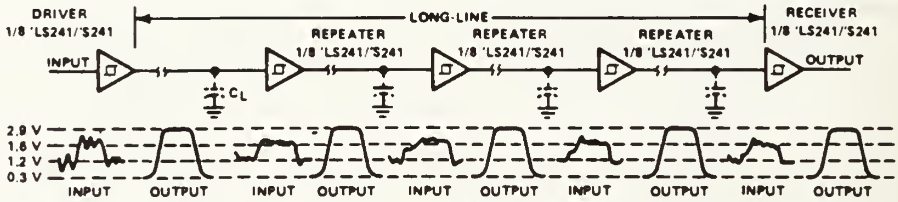
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

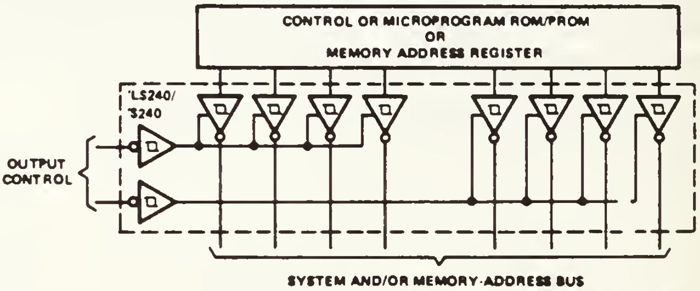
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER	TEST CONDITIONS	'S240			'S241, 'S244			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 90\ \Omega$, $C_L = 50$ pF, See Note 4		4.5	7		6	9	ns
t_{PHL}			4.5	7		6	9	ns
t_{PZL}			10	15		10	15	ns
t_{PZH}			6.5	10		8	12	ns
t_{PLZ}	$R_L = 90\ \Omega$, $C_L = 5$ pF, See Note 4		10	15		10	15	ns
t_{PHZ}			6	9		6	9	ns

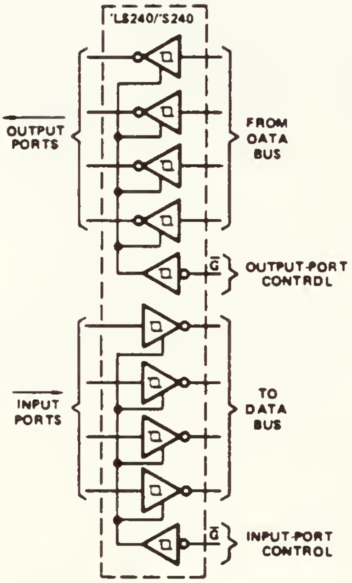
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



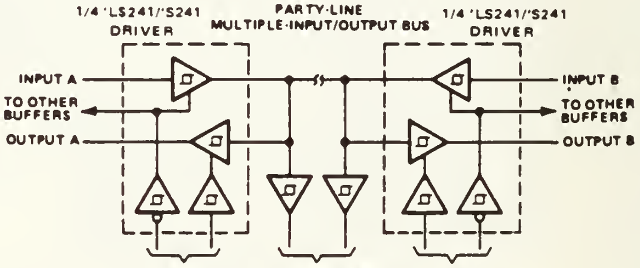
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER


CONTROL OR MICROPROGRAM ROM/PROM
OR
MEMORY ADDRESS REGISTER
'LS240/
'S240
OUTPUT
CONTROL
SYSTEM AND/OR MEMORY-ADDRESS BUS

'LS240/'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS
IN A SINGLE PACKAGE



BUS CONTROL		RECEIVERS INPUT	RECEIVERS OUTPUT	BUS CONTROL	
H	H	B	A	L	L
H	L	B	B	H	L
L	L	A	B	H	H
L	H	A	A	L	H
H	L	NONE	NONE	L	H

PARTY-LINE BUS SYSTEM
WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

APPENDIX I

DUAL MONOSTABLE MULTIVIBRATOR TECHNICAL DATA

(SNJ54LS221)

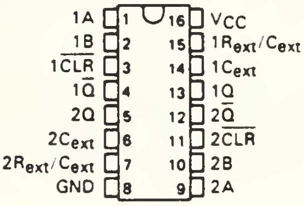
SN54221, SN54LS221, SN74221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

DECEMBER 1983 – REVISED MARCH 1988

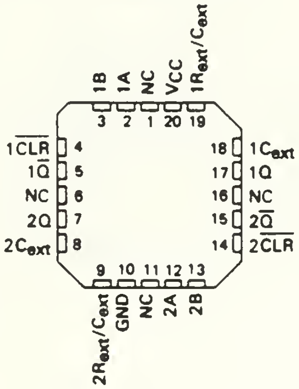
- **SN54221, SN54LS221, SN74221 and SN74LS221 Are Dual Versions of Highly Stable SN54121, SN74121 One-Shots on a Monolithic Chip**
- **SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121, SN74121 One-Shots**
- **Pin-Out Is Identical to the SN54123, SN74123, SN54LS123, SN74LS123**
- **Overriding Clear Terminates Output Pulse**

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54221	130 mW	21 s
SN74221	130 mW	28 s
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221 . . . N PACKAGE
SN74LS221 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS221 . . . FK PACKAGE
(TOP VIEW)



description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓‡	⊔‡
H	↓	H	⊓‡	⊔‡
↑†	L	H	⊓‡	⊔‡
Also see description and switching characteristics				

[†] This condition is true only if the output of the latch formed by the two NAND gates has been conditioned to the logic 1 state prior to CLR going high. This latch is conditioned by taking either A high or B low while $\overline{\text{CLR}}$ is inactive (high).

[‡] Pulsed output patterns are tested during AC switching at 25°C, with R_{ext} = 2 kΩ C_{ext} = 80 pF

description (continued)

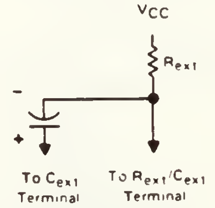
Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship $t_w(out) = C_{ext}R_{ext}\ \ln 2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device is typically less than ± 0.5% for given external timing components. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

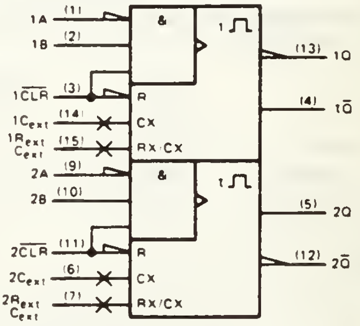
Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}, however the polarity of the capacitor will have to be changed.

TIMING COMPONENT CONNECTIONS



NOTE Due to the internal circuit, the R_{ext}/C_{ext} pin will never be more positive than the C_{ext} pin
Pin numbers shown are for D, J, N, and W packages

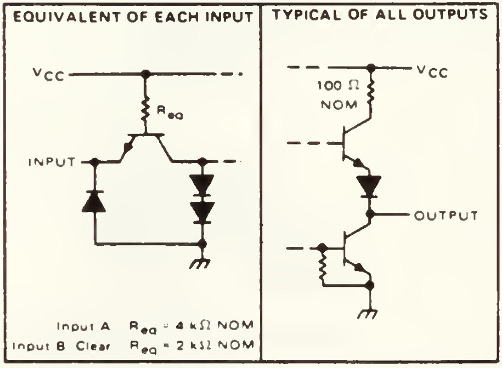
logic symbol†



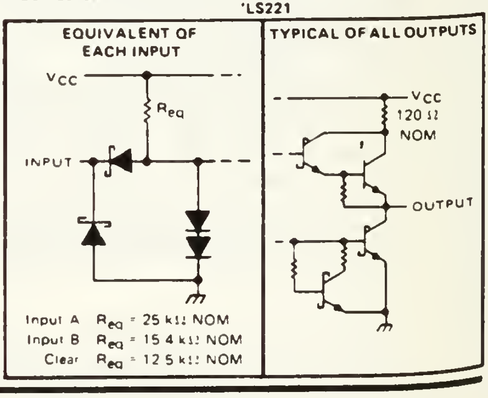
† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs

'221



'LS221



recommended operating conditions

		SN54221			SN74221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage at A input, V_{IH}		2			2			V
Low-level input voltage at A input, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	20			20			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		30	1.4		40	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_{ext} = 2 kΩ			67			67	%
	R_{ext} = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		MIN	TYP[‡]	MAX	UNIT
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	Input A			40	μA
			Input B, Clear			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Input A			−1.6	mA
			Input B, Clear			−3.2	
I_{OS}	Short-circuit output current[§]	V_{CC} = MAX	SN54221	−20		−55	mA
			SN74221	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER[†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_L = 15$ pF, $R_L = 400\ \Omega$, See Figure 1 and Note 2	$C_{ext} = 80$ pF, $R_{ext} = 2\ k\Omega$		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\bar{Q}$				50	80	ns
	B	$\bar{Q}$				40	65	
t_{PHL}	Clear	Q					27	ns
t_{PLH}	Clear	$\bar{Q}$					40	ns
$t_{w(out)}$	A or B	Q or $\bar{Q}$		$C_{ext} = 80$ pF, $R_{ext} = 2\ k\Omega$	70	110	150	ns
				$C_{ext} = 0$, $R_{ext} = 2\ k\Omega$	20	30	50	
				$C_{ext} = 100$ pF, $R_{ext} = 10\ k\Omega$	650	700	750	
				$C_{ext} = 1\ \mu F$, $R_{ext} = 10\ k\Omega$	6.5	7	7.5	ms

[†] t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
$t_{w(out)}$ ≡ Output pulse width

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS221			SN74LS221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage at A input, V_{IH}		2			2			V
Low-level input voltage at B input, V_{IL}				0.7			0.8	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	40			40			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		70	1.4		100	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_T = 2 kΩ			50			50	%
	R_T = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

recommended operating conditions

PARAMETER			TEST CONDITIONS†		SN54LS221			SN74LS221			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at B input		V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at B input		V_{CC} = MIN		0.7	0.9		0.8	0.9		V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	Input A	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
		Input B					−0.8			−0.8	
		Clear					−0.8			−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	Quiescent		4.7	11		4.7	11	mA
				Triggered		19	27		19	27	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

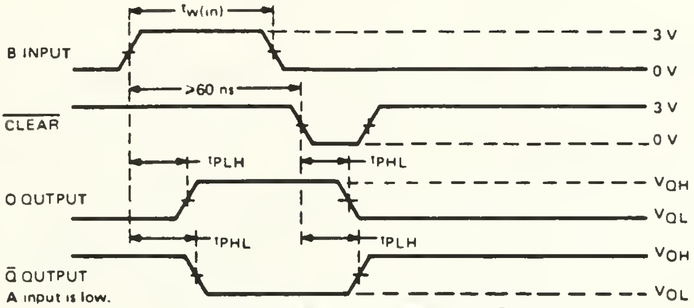
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER[†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	$C_L = 15$ pF, $R_L = 2$ kΩ, See Figure 1 and Note 3	$C_{ext} = 80$ pF, $R_{ext} = 2$ kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q				35	55	ns
t_{PLH}	Clear	$\overline{Q}$				44	65	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		$C_{ext} = 80$ pF, $R_{ext} = 2$ kΩ	70	120	150	ns
				$C_{ext} = 0$, $R_{ext} = 2$ kΩ	20	47	70	
				$C_{ext} = 100$ pF, $R_{ext} = 10$ kΩ	670	740	810	
				$C_{ext} = 1$ µF, $R_{ext} = 10$ kΩ	6	6.9	7.5	ms

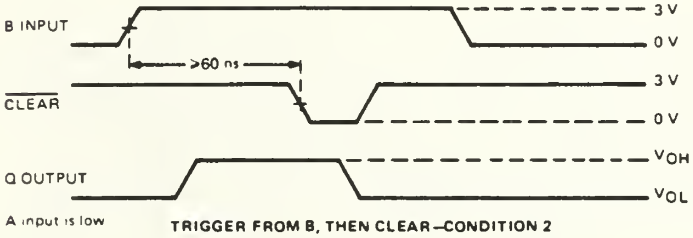
[†] t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
$t_{w(out)}$ = Output pulse width

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

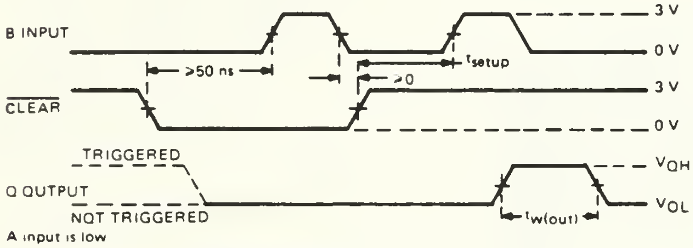
PARAMETER MEASUREMENT INFORMATION



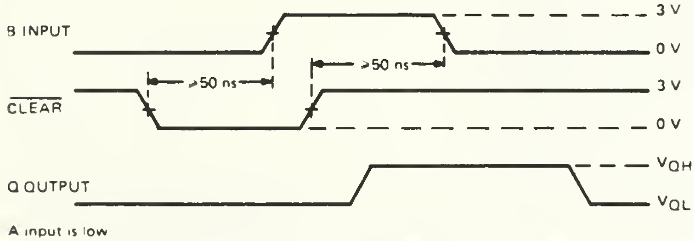
TRIGGER FROM B, THEN CLEAR—CONDITION 1



TRIGGER FROM B, THEN CLEAR—CONDITION 2



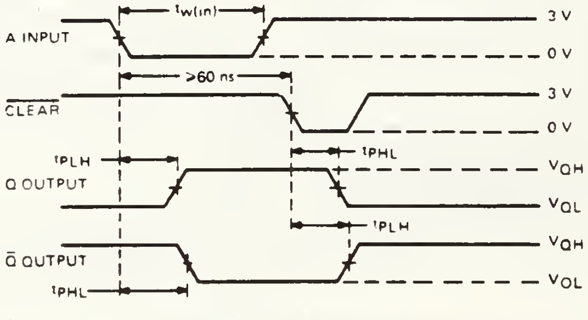
CLEAR OVERRIDING B, THEN TRIGGER FROM B



TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

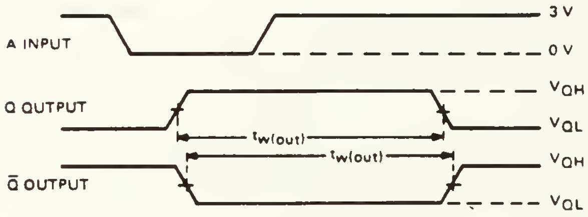
FIGURE 1—SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



B input is high

TRIGGER FROM A, THEN CLEAR



B and $\overline{\text{CLEAR}}$ inputs are high

TRIGGER FROM A

NOTES A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, for '221, $t_r \leq 7$ ns, $t_f \leq 7$ ns, for 'LS221, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. All measurements are made between the 1.5 V points of the indicated transitions for the '221 or between the 1.3 V points for the 'LS221

FIGURE 1—SWITCHING CHARACTERISTICS (CONTINUED)

TYPICAL CHARACTERISTICS ('221 ONLY)†

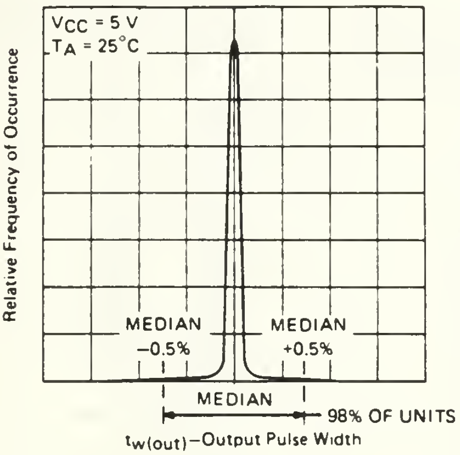

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

FIGURE 2

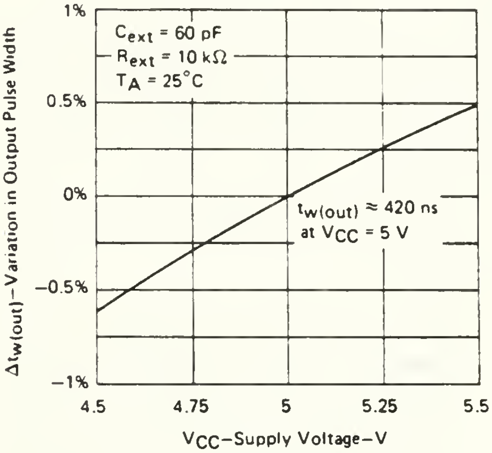

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

FIGURE 3

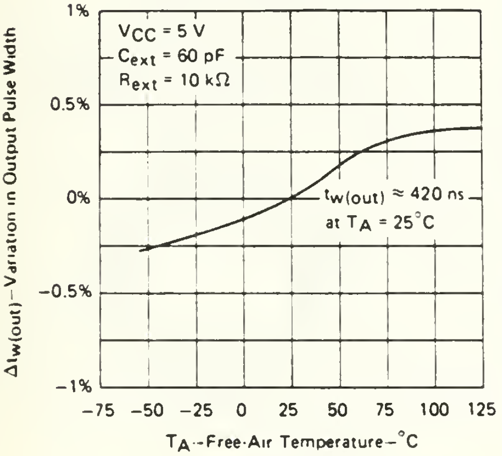

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

FIGURE 4

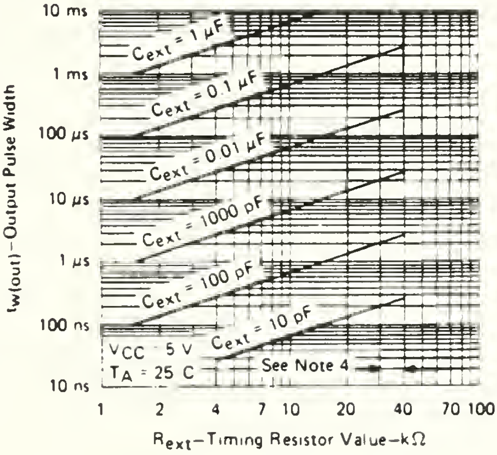

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

FIGURE 5

NOTE 4 These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221

---

† Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only

APPENDIX J

DUAL D-TYPE FLIP FLOP TECHNICAL DATA (SNJ54LS74A)

SN5474, SN54LS74A, SN54S74, SN7474, SN74LS74A, SN74S74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

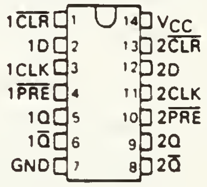
The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

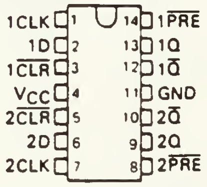
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H[†]	H[†]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

[†] The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

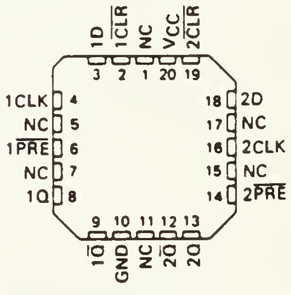
SN5474 . . . J PACKAGE
SN54LS74A, SN54S74 . . . J OR W PACKAGE
SN7474 . . . N PACKAGE
SN74LS74A, SN74S74 . . . D OR N PACKAGE
(TOP VIEW)



SN5474 . . . W PACKAGE
(TOP VIEW)

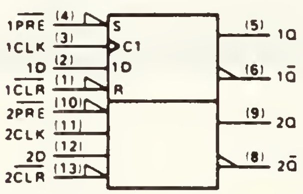


SN54LS74A, SN54S74 . . . FK PACKAGE
(TOP VIEW)



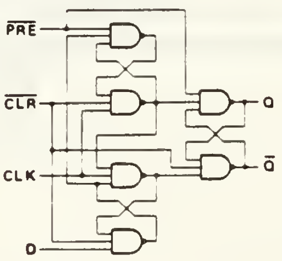
NC - No internal connection

logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

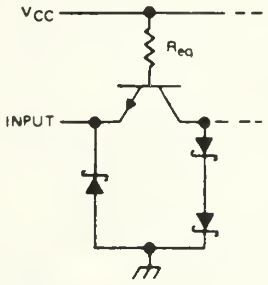
logic diagram (positive logic)



schematics of inputs and outputs

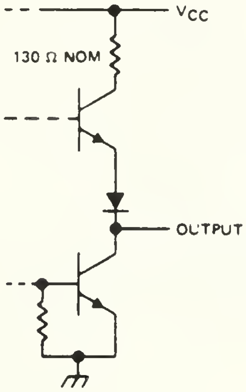
'74

EQUIVALENT OF EACH INPUT



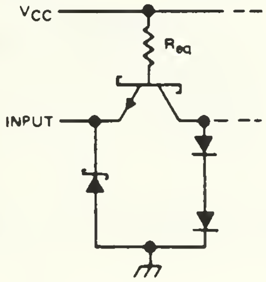
I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−3.2 mA	2 kΩ

TYPICAL OF ALL OUTPUTS



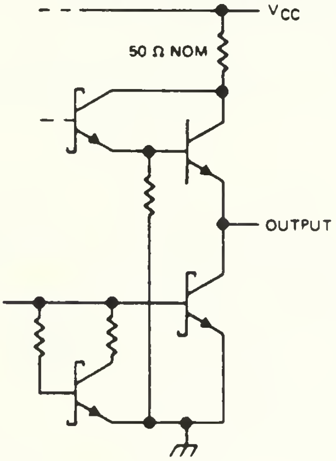
'S74

EQUIVALENT OF EACH INPUT



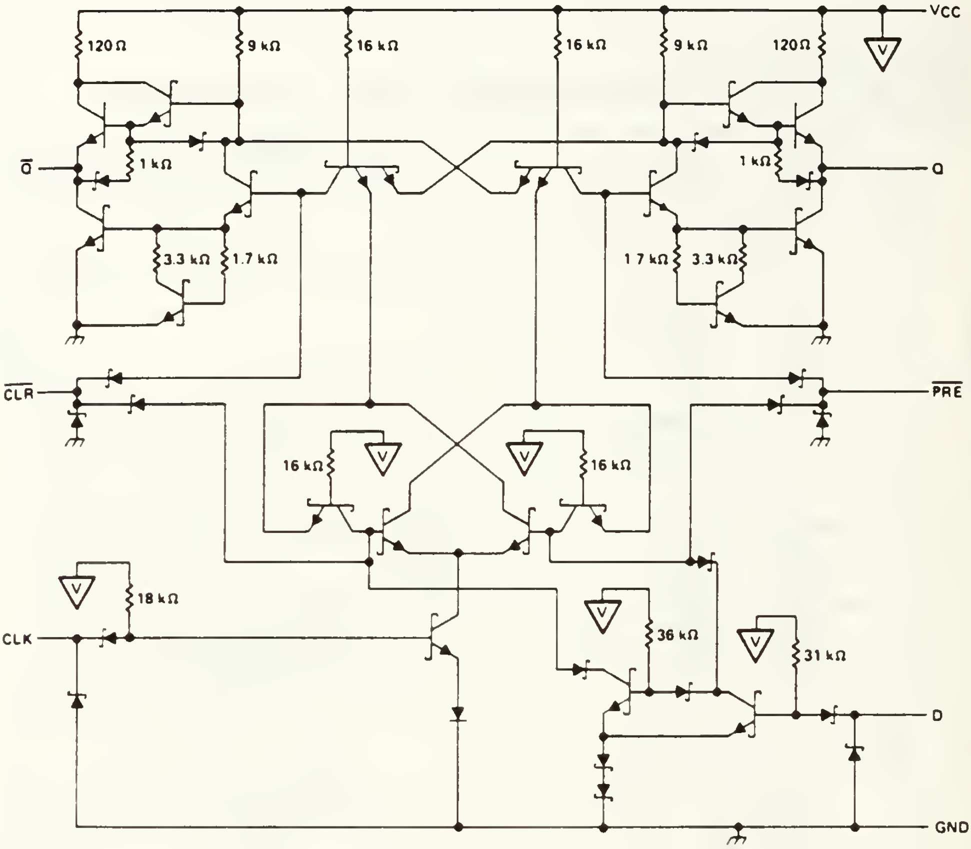
I_{IL} MAX	R_{eq} NOM
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	940 Ω

TYPICAL OF ALL OUTPUTS



schematic

'LS74A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '74, 'S74	5.5 V
'LS74A	7 V
Operating free-air temperature range: SN54'	− 55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	− 65°C to 150°C

NOTE 1 Voltage values are with respect to network ground terminal

recommended operating conditions

			SN5474			SN7474			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				16			16	mA
t_w	Pulse duration	CLK high	30			30			ns
		CLK low	37			37			
		$\overline{PRE}$ or $\overline{CLR}$ low	30			30			
t_{su}	Input setup time before CLK↑		20			20			ns
t_h	Input hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN5474			SN7474			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	D	V_{CC} = MAX, V_I = 2.4 V			40			40	µA
	$\overline{CLR}$				120			120	
	All Other				80			80	
I_{IL}	D	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
	$\overline{PRE}$[§]				−1.6			−1.6	
	$\overline{CLR}$[§]				−3.2			−3.2	
	CLK				−3.2			−3.2	
I_{OS}[¶]		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}[#]		V_{CC} = MAX, See Note 2		8.5	15		8.5	15	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C

[§] Clear is tested with preset high and preset is tested with clear high

[¶] Not more than one output should be shown at a time.

[#] Average per flip-flop

NOTE 2 With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded

switching charateristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 400 Ω, C_L = 15 pF	15	25		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$				25	ns
t_{PHL}						40	ns
t_{PLH}	CLK	Q or $\overline{Q}$			14	25	ns
t_{PHL}					20	40	ns

NOTE 3 Load circuits and voltage waveforms are shown in Section 1

recommended operating conditions

			SN54LS74A			SN74LS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration	CLK high	25			25			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	25			25			
t_{su}	Setup time before CLK↑	High-level data	20			20			ns
		Low-level data	20			20			
t_h	Hold time-data after CLK↑		5			5			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS74A			SN74LS74A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 8 mA					0.35	0.5	
I_I	D or CLK	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$				0.2			0.2	
I_{IH}	D or CLK	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$				40			40	
I_{IL}	D or CLK	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$				−0.8			−0.8	
I_{OS}§		V_{CC} = MAX, See Note 4	−20		−100	−20		−100	mA
I_{CC} (Total)		V_{CC} = MAX, See Note 2		4	8		4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2 With all outputs open, I_{CC} is measured with the Q and $\overline{\text{Q}}$ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4 For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 2 kΩ, C_L = 15 pF	25	33		MHz
t_{PLH}	$\overline{\text{CLR}}$, $\overline{\text{PRE}}$ or CLK	Q or $\overline{\text{Q}}$			13	25	ns
t_{PHL}					25	40	ns

Note 3 Load circuits and voltage waveforms are shown in Section 1.

SN54S74, SN74S74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

recommended operating conditions

			SN54S74			SN74S74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−1	mA
I_{OL}	Low-level output current				20			20	mA
t_w	Pulse duration	CLK high	6			6			ns
		CLK low	7.3			7.3			
		$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ low	7			7			
t_{su}	Setup time, before CLK↑	High-level data	3			3			ns
		Low-level data	3			3			
t_h	Input hold time - data after CLK↑		2			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54S74			SN74S74			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA,			−1.2			−1.2	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	D	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
	$\overline{\text{CLR}}$				150			150	
	$\overline{\text{PRE}}$ or CLK				100			100	
I_{IL}	D	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
	$\overline{\text{CLR}}$[¶]				−6			−6	
	$\overline{\text{PRE}}$[¶]				−4			−4	
	CLK				−4			−4	
I_{OS}[§]		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}[#]		V_{CC} = MAX, See Note 2		15	25		15	25	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

[¶] Clear is tested with preset high and preset is tested with clear high.

[#] Average per flip-flop.

NOTE 2 With all outputs open, I_{CC} is measured with the Q and $\overline{\text{Q}}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 280 Ω, C_L = 15 pF	75	110		MHz
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$			4	6	ns
t_{PHL}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK high)	$\overline{\text{Q}}$ or Q			9	13.5	ns
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK low)				5	8	
t_{PLH}	CLK	Q or $\overline{\text{Q}}$			6	9	ns
t_{PHL}					6	9	ns

NOTE 3 Load circuits and voltage waveforms are shown in Section 1.

APPENDIX K

QUADRUPLE POSITIVE NAND GATE TECHNICAL DATA

(SNJ54LS00)

SN5400, SN54LS00, SN54S00, SN7400, SN74LS00, SN74S00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

DECEMBER 1983 - REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

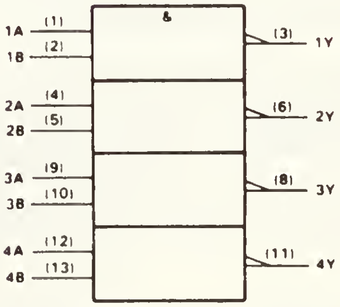
These devices contain four independent 2-input-NAND gates.

The SN5400, SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7400, SN74LS00, and SN74S00 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

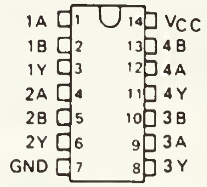
logic symbol[†]



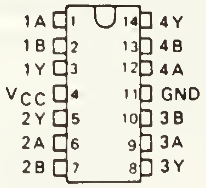
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

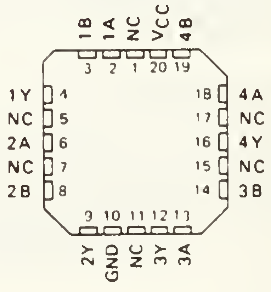
SN5400 . . . J PACKAGE
SN54LS00, SN54S00 . . . J OR W PACKAGE
SN7400 . . . N PACKAGE
SN74LS00, SN74S00 . . . D OR N PACKAGE
(TOP VIEW)



SN5400 . . . W PACKAGE
(TOP VIEW)

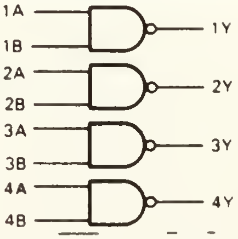


SN54LS00, SN54S00 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

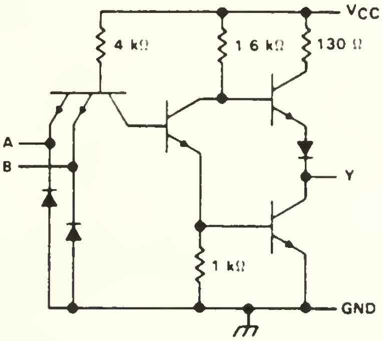
logic diagram (positive logic)



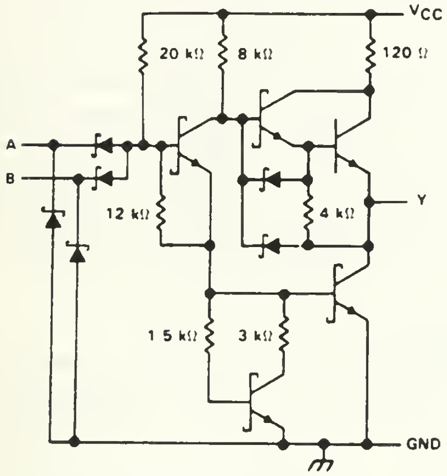
$Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

schematics (each gate)

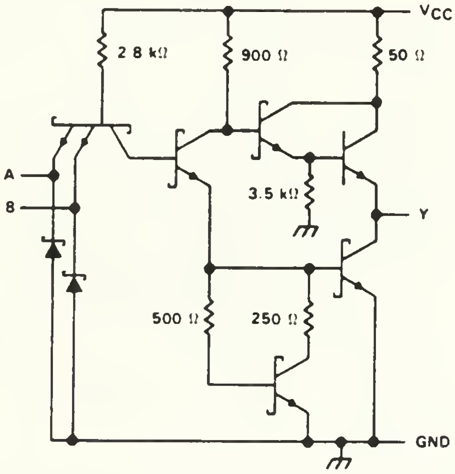
'00



'LS00



'S00



Resistor values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage:	'00, 'S00	5.5 V
	'LS00	7 V
Operating free-air temperature range:	SN54'	−55 °C to 125 °C
	SN74'	0 °C to 70 °C
Storage temperature range		−65 °C to 150 °C

NOTE 1 Voltage values are with respect to network ground terminal

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN5400			SN7400			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5400			SN7400			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, $I_I = -12$ mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, $V_{IL} = 0.8$ V, $I_{OH} = -0.4$ mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, $V_{IH} = 2$ V, $I_{OL} = 16$ mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, $V_I = 5.5$ V			1			1	mA
I_{IH}	V_{CC} = MAX, $V_I = 2.4$ V			40			40	μA
I_{IL}	V_{CC} = MAX, $V_I = 0.4$ V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, $V_I = 0$ V		4	8		4	8	mA
I_{CCL}	V_{CC} = MAX, $V_I = 4.5$ V		12	22		12	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 400\ \Omega$, $C_L = 15$ pF		11	22	ns
t_{PHL}					7	15	ns

NOTE 2 Load circuits and voltage waveforms are shown in Section 1.

SN54LS00, SN74LS00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

recommended operating conditions

		SN54LS00			SN74LS00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN54LS00			SN74LS00			UNIT
				MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN	V_{IL} = MAX	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	$_{H}$ = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			2.4	4.4		2.4	4.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ,	C_L = 15 pF		9	15	ns
t_{PHL}						10	15	ns

NOTE 2. Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54S00			SN74S00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54S00			SN74S00			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			50			50	µA
I_{IL}	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS} [§]	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		10	16		10	16	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5 V		20	36		20	36	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω,	C_L = 15 pF		3	4.5	ns
t_{PHL}						3	5	ns
t_{PLH}			R_L = 280 Ω,	C_L = 50 pF		4.5		ns
t_{PHL}						5		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

APPENDIX L

SUMMARY OF DATA WORDS LOST FROM ORIGINAL MUSTANG FLIGHT DATA

Word in Spectrum	Wavelength Å		Words Lost
1	1800.000	1	
2	1803.133	2	
3	1806.266	3	
4	1809.399	4	
5	1812.532	5	
6	1815.665	6	
7	1818.798	7	
8	1821.931	8	
9	1825.064	9	
10	1828.197	10	
11	1831.330	11	
12	1834.463	12	
13	1837.596	13	
14	1840.729	14	
15	1843.862	15	
16	1846.995	16	
17	1850.128		1
18	1853.261	1	
19	1856.394	2	
20	1859.527	3	
21	1862.660	4	
22	1865.793	5	
23	1868.926	6	
24	1872.059	7	
25	1875.192	8	
26	1878.325	9	
27	1881.458	10	
28	1884.591	11	
29	1887.724	12	
30	1890.857	13	
31	1893.990	14	
32	1897.123	15	
33	1900.256	16	
34	1903.389		2
35	1906.522	1	
36	1909.655	2	
37	1912.788	3	
38	1915.921	4	
39	1919.054	5	
40	1922.187	6	

41	1925.320	7	
42	1928.453	8	
43	1931.586	9	
44	1934.719	10	
45	1937.852	11	
46	1940.985	12	
47	1944.118	13	
48	1947.251	14	
49	1950.384	15	
50	1953.517	16	
51	1956.650		3
52	1959.783	1	
53	1962.916	2	
54	1966.049	3	
55	1969.182	4	
56	1972.315	5	
57	1975.448	6	
58	1978.581	7	
59	1981.714	8	
60	1984.847	9	
61	1987.980	10	
62	1991.113	11	
63	1994.246	12	
64	1997.379	13	
65	2000.512	14	
66	2003.645	15	
67	2006.778	16	
68	2009.911		4
69	2013.044	1	
70	2016.177	2	
71	2019.310	3	
72	2022.443	4	
73	2025.576	5	
74	2028.709	6	
75	2031.842	7	
76	2034.975	8	
77	2038.108	9	
78	2041.241	10	
79	2044.374	11	
80	2047.507	12	
81	2050.640	13	
82	2053.773	14	
83	2056.906	15	
84	2060.039	16	
85	2063.172		5
86	2066.305	1	
87	2069.438	2	
88	2072.571	3	
89	2075.704	4	
90	2078.837	5	
91	2081.970	6	

92	2085.103	7	
93	2088.236	8	
94	2091.369	9	
95	2094.502	10	
96	2097.635	11	
97	2100.768	12	
98	2103.901	13	
99	2107.034	14	
100	2110.167	15	
101	2113.300	16	
102	2116.433		6
103	2119.566		7
104	2122.699	1	
105	2125.832	2	
106	2128.965	3	
107	2132.098	4	
108	2135.231	5	
109	2138.364	6	
110	2141.497	7	
111	2144.630	8	
112	2147.763	9	
113	2150.896	10	
114	2154.029	11	
115	2157.162	12	
116	2160.295	13	
117	2163.428	14	
118	2166.561	15	
119	2169.694	16	
120	2172.827		8
121	2175.960	1	
122	2179.093	2	
123	2182.226	3	
124	2185.359	4	
125	2188.492	5	
126	2191.625	6	
127	2194.758	7	
128	2197.891	8	
129	2201.024	9	
130	2204.157	10	
131	2207.290	11	
132	2210.423	12	
133	2213.556	13	
134	2216.689	14	
135	2219.822	15	
136	2222.955	16	
137	2226.088		9
138	2229.221	1	
139	2232.354	2	
140	2235.487	3	
141	2238.620	4	
142	2241.753	5	

143	2244.886	6	
144	2248.019	7	
145	2251.152	8	
146	2254.285	9	
147	2257.418	10	
148	2260.551	11	
149	2263.684	12	
150	2266.817	13	
151	2269.950	14	
152	2273.083	15	
153	2276.216	16	
154	2279.349		10
155	2282.482	1	
156	2285.615	2	
157	2288.748	3	
158	2291.881	4	
159	2295.014	5	
160	2298.147	6	
161	2301.280	7	
162	2304.413	8	
163	2307.546	9	
164	2310.679	10	
165	2313.812	11	
166	2316.945	12	
167	2320.078	13	
168	2323.211	14	
169	2326.344	15	
170	2329.477	16	
171	2332.610		11
172	2335.743	1	
173	2338.876	2	
174	2342.009	3	
175	2345.142	4	
176	2348.275	5	
177	2351.408	6	
178	2354.541	7	
179	2357.674	8	
180	2360.807	9	
181	2363.940	10	
182	2367.073	11	
183	2370.206	12	
184	2373.339	13	
185	2376.472	14	
186	2379.605	15	
187	2382.738	16	
188	2385.871		12
189	2389.004	1	
190	2392.137	2	
191	2395.270	3	
192	2398.403	4	
193	2401.536	5	

194	2404.669	6	
195	2407.802	7	
196	2410.935	8	
197	2414.068	9	
198	2417.201	10	
199	2420.334	11	
200	2423.467	12	
201	2426.600	13	
202	2429.733	14	
203	2432.866	15	
204	2435.999	16	
205	2439.132		13
206	2442.265	1	
207	2445.398	2	
208	2448.531	3	
209	2451.664	4	
210	2454.797	5	
211	2457.930	6	
212	2461.063	7	
213	2464.196	8	
214	2467.329	9	
215	2470.462	10	
216	2473.595	11	
217	2476.728	12	
218	2479.861	13	
219	2482.994	14	
220	2486.127	15	
221	2489.260	16	
222	2492.393		14
223	2495.526	1	
224	2498.659	2	
225	2501.792	3	
226	2504.925	4	
227	2508.058	5	
228	2511.191	6	
229	2514.324	7	
230	2517.457	8	
231	2520.590	9	
232	2523.723	10	
233	2526.856	11	
234	2529.989	12	
235	2533.122	13	
236	2536.255	14	
237	2539.388	15	
238	2542.521	16	
239	2545.654		15
240	2548.787		16
241	2551.920	1	
242	2555.053	2	
243	2558.186	3	
244	2561.319	4	

245	2564.452	5	
246	2567.585	6	
247	2570.718	7	
248	2573.851	8	
249	2576.984	9	
250	2580.117	10	
251	2583.250	11	
252	2586.383	12	
253	2589.516	13	
254	2592.649	14	
255	2595.782	15	
256	2598.915	16	
257	2602.048	1	
258	2605.181	2	
259	2608.314	3	
260	2611.447	4	
261	2614.580	5	
262	2617.713	6	
263	2620.846	7	
264	2623.979	8	
265	2627.112	9	
266	2630.245	10	
267	2633.378	11	
268	2636.511	12	
269	2639.644	13	
270	2642.777	14	
271	2645.910	15	
272	2649.043	16	
273	2652.176		17
274	2655.309	1	
275	2658.442	2	
276	2661.575	3	
277	2664.708	4	
278	2667.841	5	
279	2670.974	6	
280	2674.107	7	
281	2677.240	8	
282	2680.373	9	
283	2683.506	10	
284	2686.639	11	
285	2689.772	12	
286	2692.905	13	
287	2696.038	14	
288	2699.171	15	
289	2702.304	16	
290	2705.437		18
291	2708.570	1	
292	2711.703	2	
293	2714.836	3	
294	2717.969	4	
295	2721.102	5	

296	2724.235	6	
297	2727.368	7	
298	2730.501	8	
299	2733.634	9	
300	2736.767	10	
301	2739.900	11	
302	2743.033	12	
303	2746.166	13	
304	2749.299	14	
305	2752.432	15	
306	2755.565	16	
307	2758.698		19
308	2761.831	1	
309	2764.964	2	
310	2768.097	3	
311	2771.230	4	
312	2774.363	5	
313	2777.496	6	
314	2780.629	7	
315	2783.762	8	
316	2786.895	9	
317	2790.028	10	
318	2793.161	11	
319	2796.294	12	
320	2799.427	13	
321	2802.560	14	
322	2805.693	15	
323	2808.826	16	
324	2811.959		20
325	2815.092	1	
326	2818.225	2	
327	2821.358	3	
328	2824.491	4	
329	2827.624	5	
330	2830.757	6	
331	2833.890	7	
332	2837.023	8	
333	2840.156	9	
334	2843.289	10	
335	2846.422	11	
336	2849.555	12	
337	2852.688	13	
338	2855.821	14	
339	2858.954	15	
340	2862.087	16	
341	2865.220		21
342	2868.353	1	
343	2871.486	2	
344	2874.619	3	
345	2877.752	4	
346	2880.885	5	

347	2884.018	6	
348	2887.151	7	
349	2890.284	8	
350	2893.417	9	
351	2896.550	10	
352	2899.683	11	
353	2902.816	12	
354	2905.949	13	
355	2909.082	14	
356	2912.215	15	
357	2915.348	16	
358	2918.481		22
359	2921.614	1	
360	2924.747	2	
361	2927.880	3	
362	2931.013	4	
363	2934.146	5	
364	2937.279	6	
365	2940.412	7	
366	2943.545	8	
367	2946.678	9	
368	2949.811	10	
369	2952.944	11	
370	2956.077	12	
371	2959.210	13	
372	2962.343	14	
373	2965.476	15	
374	2968.609	16	
375	2971.742		23
376	2974.875		24
377	2978.008	1	
378	2981.141	2	
379	2984.274	3	
380	2987.407	4	
381	2990.540	5	
382	2993.673	6	
383	2996.806	7	
384	2999.939	8	
385	3003.072	9	
386	3006.205	10	
387	3009.338	11	
388	3012.471	12	
389	3015.604	13	
390	3018.737	14	
391	3021.870	15	
392	3025.003	16	
393	3028.136		25
394	3031.269	1	
395	3034.402	2	
396	3037.535	3	
397	3040.668	4	

398	3043.801	5	
399	3046.934	6	
400	3050.067	7	
401	3053.200	8	
402	3056.333	9	
403	3059.466	10	
404	3062.599	11	
405	3065.732	12	
406	3068.865	13	
407	3071.998	14	
408	3075.131	15	
409	3078.264	16	
410	3081.397		26
411	3084.530	1	
412	3087.663	2	
413	3090.796	3	
414	3093.929	4	
415	3097.062	5	
416	3100.195	6	
417	3103.328	7	
418	3106.461	8	
419	3109.594	9	
420	3112.727	10	
421	3115.860	11	
422	3118.993	12	
423	3122.126	13	
424	3125.259	14	
425	3128.392	15	
426	3131.525	16	
427	3134.658		27
428	3137.791	1	
429	3140.924	2	
430	3144.057	3	
431	3147.190	4	
432	3150.323	5	
433	3153.456	6	
434	3156.589	7	
435	3159.722	8	
436	3162.855	9	
437	3165.988	10	
438	3169.121	11	
439	3172.254	12	
440	3175.387	13	
441	3178.520	14	
442	3181.653	15	
443	3184.786	16	
444	3187.919		28
445	3191.052	1	
446	3194.185	2	
447	3197.318	3	
448	3200.451	4	

449	3203.584	5	
450	3206.717	6	
451	3209.850	7	
452	3212.983	8	
453	3216.116	9	
454	3219.249	10	
455	3222.382	11	
456	3225.515	12	
457	3228.648	13	
458	3231.781	14	
459	3234.914	15	
460	3238.047	16	
461	3241.180		29
462	3244.313	1	
463	3247.446	2	
464	3250.579	3	
465	3253.712	4	
466	3256.845	5	
467	3259.978	6	
468	3263.111	7	
469	3266.244	8	
470	3269.377	9	
471	3272.510	10	
472	3275.643	11	
473	3278.776	12	
474	3281.909	13	
475	3285.042	14	
476	3288.175	15	
477	3291.308	16	
478	3294.441		30
479	3297.574	1	
480	3300.707	2	
481	3303.840	3	
482	3306.973	4	
483	3310.106	5	
484	3313.239	6	
485	3316.372	7	
486	3319.505	8	
487	3322.638	9	
488	3325.771	10	
489	3328.904	11	
490	3332.037	12	
491	3335.170	13	
492	3338.303	14	
493	3341.436	15	
494	3344.569	16	
495	3347.702		31
496	3350.835	1	
497	3353.968	2	
498	3357.101	3	
499	3360.234	4	

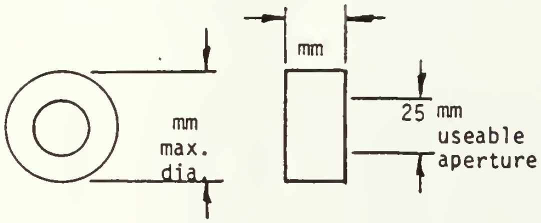
500	3363.367	5	
501	3366.500	6	
502	3369.633	7	
503	3372.766	8	
504	3375.899	9	
505	3379.032	10	
506	3382.165	11	
507	3385.298	12	
508	3388.431	13	
509	3391.564	14	
510	3394.697	15	
511	3397.830	16	
512	3400.963		32

APPENDIX M

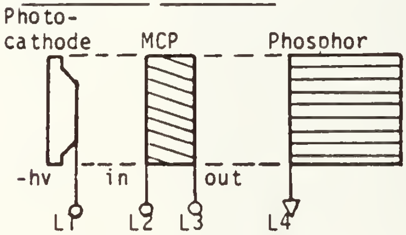
ITT IMAGE INTENSIFIER TECHNICAL DATA

ITT
ELECTRO-OPTICAL
PRODUCTS DIVISION
3700 East Pontiac Street
P.O. Box 3700
Fort Wayne, Indiana 46801

1.0 OUTLINE DRAWINGS



2.0 ELECTRICAL SCHEMATIC



3.0 LEAD CONNECTIONS

LEAD	COLOR	ELEMENT	
1	Blue	Photocathode	(neg.)
2	Red	MCP Input	(neg.)
3	Orange	MCP Output	(neg.)
4	Yellow	Phosphor	(ground)

4.0 MAXIMUM OPERATING VOLTAGES *

Cathode to MCP input 180 volts
MCP input to MCP output 1820 volts
MCP output to Phosphor 6000 volts
* voltages for 50,000 e gain

4.1 USE WITH POWER SUPPLY

Model # 200057 S/N 0105

-DATA SHEET 1-

-PROXIMITY FOCUSED CHANNEL INTENSIFIER TUBE-

TUBE S/N XXH0967
TUBE TYPE F4145
CsTe/F.S.; P20/FO
DATE 06/91

5.0 CATHODE SENSITIVITY

- ua/lumen

6.0 RESOLUTION

- lp/mm
@ - MCP volts

7.0 LUMINOUS GAIN

-

8.0 GAIN UNIFORMITY

13 %
@ 50 K e gain

9.0 EQUIVALENT BACKGROUND INPUT

- lumens/cm^2
@ - gain

10.0 MCP VOLTAGE

Set for 1820V at 10V Control

-DATA SHEET 2-

-PROXIMITY FOCUSED CHANNEL INTENSIFIER TUBE-

Tube S/N XXH0967 Tube Type F4145 Date 02/90

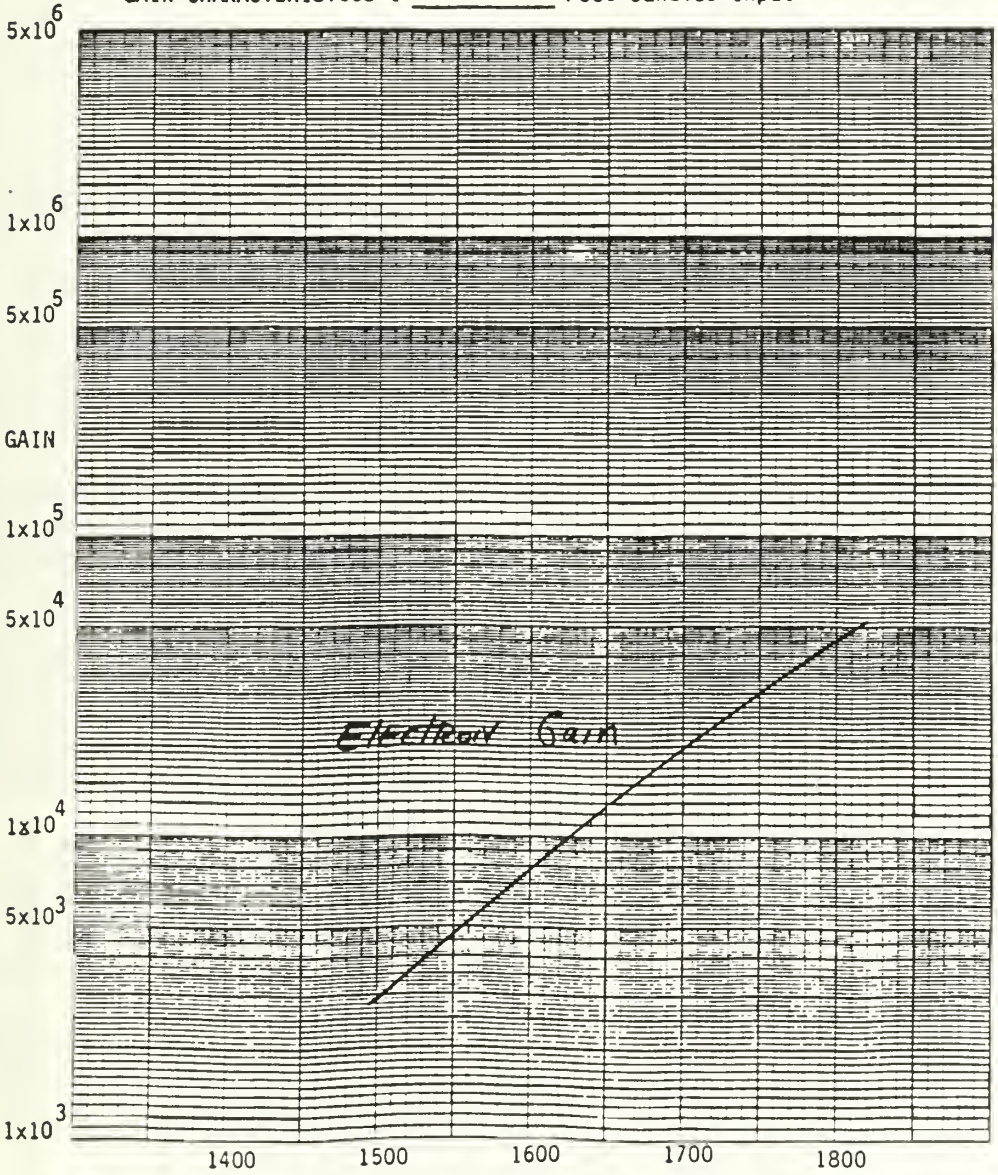
MCP Conductivity 1.1×10^{-5} amps @ 1000 volts

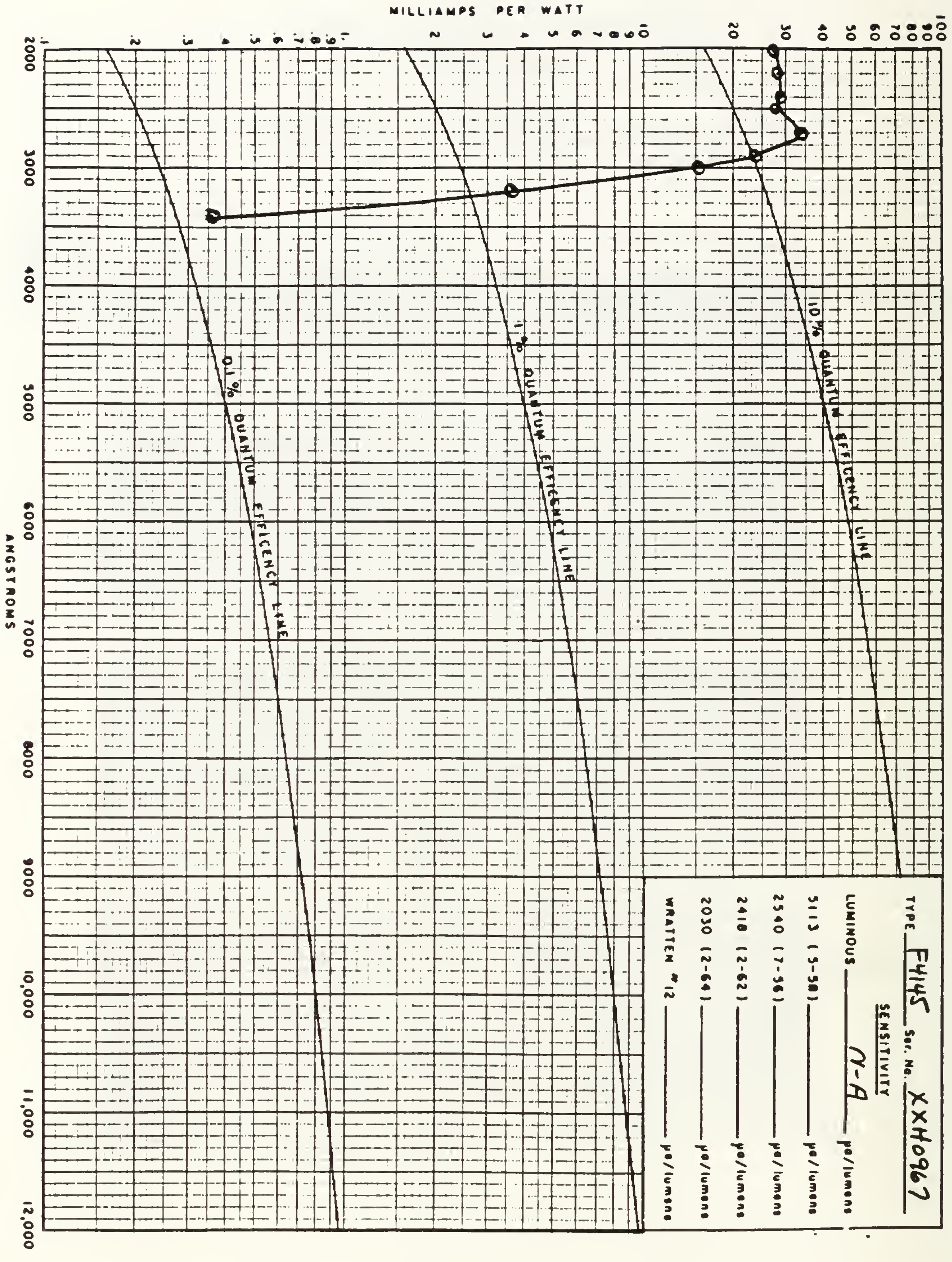
Photocathode Sensitivity — ua/L @ — Lumens

Photocathode Type/Window CsTe/F.S. Phosphor Type P20

Photocathode Voltage 180 Phosphor Voltage 6000

GAIN CHARACTERISTICS @ UV Foot-Candles Input




MILLIAMPS PER WATT
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90
100
ANGSTROMS
2000
3000
4000
5000
6000
7000
8000
9000
10,000
11,000
12,000
0.1 % QUANTUM EFFICENCY LINE
1 % QUANTUM EFFICENCY LINE
10 % QUANTUM EFFICENCY LINE
TYPE F4145 Ser. No. XXH0967
SENSITIVITY
LUMINOUS N-A μa/lumens
5113 (5-58) μa/lumens
2540 (7-56) μa/lumens
2418 (2-62) μa/lumens
2030 (2-64) μa/lumens
WRATTEN #12 μa/lumens

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